APPLICATION MANUAL

RV-8523

Real Time Clock / Calendar Module

with I2C Interface

A COMPANY OF THE SWATCH GROUP

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RV-8523

I²C-Bus Interface Real Time Clock / Calendar Module

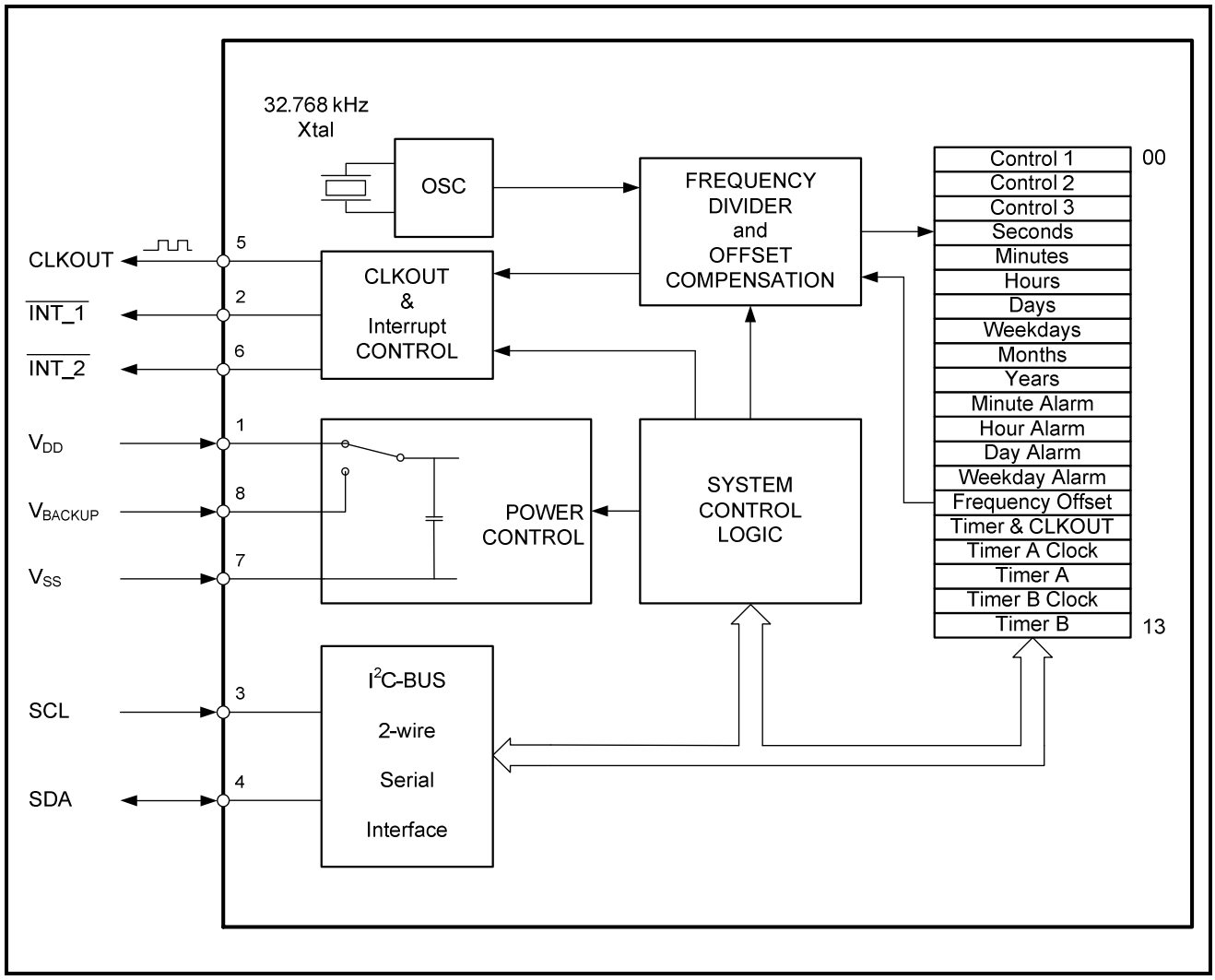
1. OVERVIEW

- RTC module with built-in crystal oscillating at 32.768 kHz
- 1 MHz Fast-mode Plus (Fm+) two-wire I²C interface
- Wide Interface operating voltage: 1.6 – 5.5 V
- Wide clock operating voltage: 1.2 – 5.5 V
- Ultra low power consumption: 130 nA typ @ 3.0V / 25°C
- Provides year, month, day, weekday, hours, minutes, seconds
- Freely programmable Alarm and Timer functions with interrupt capability
- Low voltage detector, internal power on reset
- Battery backup input pin and switch-over circuit
- $\overline{\text{INT\_1}}$ can be programed either as interrupt or clock output (open-drain)
- Programmable clock output for peripheral devices (32.768 kHz, 16.384 kHz, 8192 Hz, 4096 Hz, 1024 Hz, 32 Hz and 1 Hz)
- Programmable offset register for frequency adjustment
- I²C slave address: read D1h, write D0h
- Available in small and compact package size, RoHS-compliant and 100% leadfree:
  C3: 3.7 x 2.5 x 0.9 mm

2. GENERAL DESCRIPTION

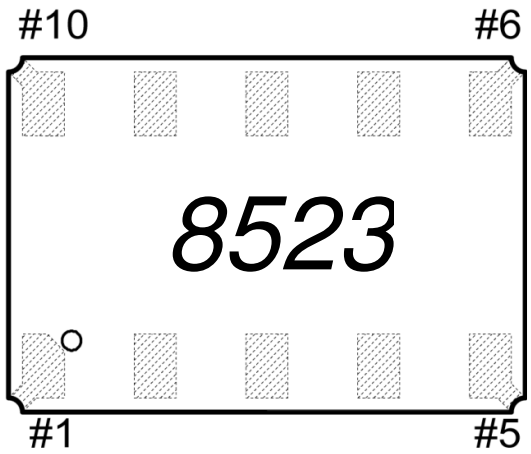
The RV-8523 is a CMOS real time clock / calendar optimized for low power consumption. Data is transferred serially via an I²C bus with a maximum data rate of 1000 kbit/s. Alarm and timer functions are available with the possibility to generate a wake-up signal on an interrupt pin. An offset register allows fine-tuning of the clock. The RV-8523 has a backup battery switch-over circuit, which detects power failures and automatically switches to the battery supply when a power failure occurs.

3. BLOCK DIAGRAM



4. PINOUT

C3 Package:



#1	V_{DD}	#10	N.C.
#2	$\overline{INT\_1}$	#9	N.C.
#3	SCL	#8	V_{BACKUP}
#4	SDA	#7	V_{SS}
#5	CLKOUT	#6	$\overline{INT\_2}$

5. PIN DESCRIPTION

Symbol	Pin #	Description
V_{DD}	1	Power Supply Voltage
$\overline{INT\_1}$	2	Interrupt_1 Output pin (active LOW) / Clock Output pin; open-drain; requires pull-up resistor
SCL	3	Serial Clock Input pin; requires pull-up resistor
SDA	4	Serial Data Input-Output pin; requires pull-up resistor
CLKOUT	5	Clock Output pin; open-drain; requires pull-up resistor
$\overline{INT\_2}$	6	Interrupt_2 Output pin (active LOW); open-drain; requires pull-up resistor
V_{SS}	7	Ground
V_{BACKUP}	8	Backup Supply Voltage; tie to GND when not using backup supply voltage
N.C.	9	Not Connected
N.C.	10	Not Connected

6. FUNCTIONAL DESCRIPTION

The RV-8523 RTC module combines a RTC IC with on chip oscillator together with a 32.768 kHz quartz crystal in a miniature ceramic package.

The RV-8523 contains:

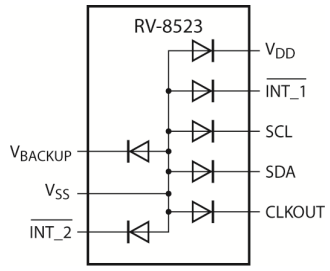
- 20 8-bit registers with an auto-incrementing address register
- A frequency divider, which provides the source clock for the real time clock (RTC)
- A programmable clock output
- A 1 Mbit/s I^2C bus interface
- An offset register, which allows fine-tuning of the clock

All 20 registers are designed as addressable 8-bit registers although not all bits are implemented:

- The first three registers (memory address 00h, 01h, and 02h) are used as control and status registers
- The addresses 03h through 09h are used as counters for the clock function (seconds up to years)
- Addresses 0Ah through 0Dh define the alarm condition
- Address 0Eh defines the offset calibration
- Address 0Fh defines the clock-out mode and the addresses 10h and 12h the timers mode
- Addresses 11h and 13h are used for the timers

The registers Seconds, Minutes, Hours, Days, Weekdays, Months, and Years are all coded in Binary Coded Decimal (BCD) format. Other registers are either bit-wise or standard binary. When one of the RTC registers is read, the contents of all counters are frozen. Therefore, faulty reading of the clock and calendar during a carry condition is prevented.
The RV-8523 has a battery backup input pin and battery switch-over circuit, which monitors the main power supply and automatically switches to the backup battery when a power failure condition is detected. Accurate timekeeping is maintained even when the main power supply is interrupted.
A battery low detection circuit monitors the status of the battery. When the battery voltage goes below a certain threshold value, a flag is set to indicate that the battery must be replaced soon. This ensures the integrity of the data during periods of battery backup.

7. DEVICE PROTECTION DIAGRAM

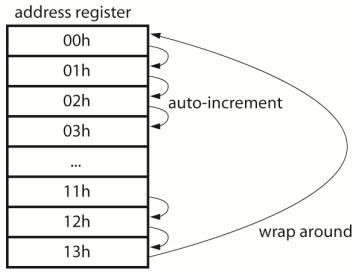


8. REGISTER ORGANIZATION

8.1. REGISTER OVERVIEW

The 20 registers of the RV-8523 are auto-incrementing after each read or write data byte up to register 13h. After register 13h, the auto-incrementing will wrap around to address 00h.

Auto-incrementing of the registers:



Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	Control 1	CAP	N	STOP	SR	12_24	SIE	AIE	CIE
01h	Control 2	WTAF	CTAF	CTBF	SF	AF	WTAIE	CTAIE	CTBIE
02h	Control 3	PM2	PM1	PM0	X	BSF	BLF	BSIE	BLIE
03h	Seconds	OS	40	20	10	8	4	2	1
04h	Minutes	X	40	20	10	8	4	2	1
05h	Hours in 12 h mode	X	X	AMPM	10	8	4	2	1
	Hours in 24 h mode	X	X	20	10	8	4	2	1
06h	Days	X	X	20	10	8	4	2	1
07h	Weekdays	X	X	X	X	X	4	2	1
08h	Months	X	X	X	10	8	4	2	1
09h	Years	80	40	20	10	8	4	2	1
0Ah	Minute Alarm	AE_M	40	20	10	8	4	2	1
0Bh	Hour Alarm in 12 h mode	AE_H	X	AMPM	10	8	4	2	1
	Hour Alarm in 24 h mode	AE_H	X	20	10	8	4	2	1
0Ch	Day Alarm	AE_D	X	20	10	8	4	2	1
0Dh	Weekday Alarm	AE_W	X	X	X	X	4	2	1
0Eh	Frequency Offset	MODE	Offset value						
0Fh	Timer & CLKOUT	TAM	TBM	COF2	COF1	COF0	TAC1	TAC0	TBC
10h	Timer A Clock	X	X	X	X	X	TAQ2	TAQ1	TAQ0
11h	Timer A	128	64	32	16	8	4	2	1
12h	Timer B Clock	X	TBW2	TBW1	TBW0	X	TBQ2	TBQ1	TBQ0
13h	Timer B	128	64	32	16	8	4	2	1

Bit positions labeled as “X” are not implemented and will return 0 when read.
Bit position labeled as “N” must always be written with logic 0.

8.2. CONTROL REGISTERS

8.2.1.CONTROL 1 (address 00h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	Control 1	CAP	N	STOP	SR	12_24	SIE	AIE	CIE

Bit	Symbol	Value	Description	Reference
7	CAP	0[1)]	Must be set to logic 0 for normal operations	
6	N	0[1) 2)]	Unused	
5	STOP	0[1)]	RTC time circuits running	
		1	RTC time circuits frozen RTC divider chain flip-flops are asynchronously set to logic 0 CLKOUT at 32.768 kHz, 16.384 kHz, or 8.192 kHz is still available	
4	SR	0[1) 3)]	No software reset	
		1	Initiate software reset	
3	12_24	0[1)]	24 hour mode is selected	
		1	12 hour mode is selected	
2	SIE	0[1)]	Second interrupt disabled	
		1	Second interrupt enabled	
1	AIE	0[1)]	Alarm interrupt disabled	
		1	Alarm interrupt enabled	
0	CIE	0[1)]	No correction interrupt generated	See section 8.5.
		1	Interrupt pulses are generated at every correction cycles	

[1)] Default value.
[2)] Bit labeled as “N” must always be written with logic 0.
[3)] For a software reset, 01011000 (58h) must be sent to register Control 1 (see section 8.7.). Bit SR always returns 0 when read.

8.2.2.CONTROL 2 (address 01h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01h	Control 2	WTAF	CTAF	CTBF	SF	AF	WTAIE	CTAIE	CTBIE

Bit	Symbol	Value	Description	Reference
7	WTAF	0[1)]	No watchdog timer A interrupt generated	
		1	Flag set when watchdog timer A interrupt generated Flag is read-only and cleared by reading register Control 2	
6	CTAF	0[1)]	No countdown timer A interrupt generated	
		1	Flag set when countdown timer A interrupt generated Flag must be cleared to clear interrupt	
5	CTBF	0[1)]	No countdown timer B interrupt generated	
		1	Flag set when countdown timer B interrupt generated Flag must be cleared to clear interrupt	
4	SF	0[1)]	No second interrupt generated	
		1	Flag set when second interrupt generated Flag must be cleared to clear interrupt	
3	AF	0[1)]	No alarm interrupt generated	
		1	Flag set when alarm triggered Flag must be cleared to clear interrupt	
2	WTAIE	0[1)]	Watchdog timer A interrupt is disabled	
		1	Watchdog timer A interrupt is enabled	
1	CTAIE	0[1)]	Countdown timer A interrupt is disabled	
		1	Countdown timer A interrupt is enabled	
0	CTBIE	0[1)]	Countdown timer B interrupt is disabled	
		1	Countdown timer B interrupt is enabled	

[1)] Default value.

8.2.3.CONTROL 3 (address 02h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
02h	Control 3	PM2	PM1	PM0	X	BSF	BLF	BSIE	BLIE

Bit	Symbol	Value	Description	Reference
7 to 5	PM[2:0]	000 to 111	Battery switchover and battery low detection control[1)]	See section 9.2.
4	X	-	Unused	
3	BSF	0[2)]	No battery switchover interrupt generated	
		1	Flag set when battery switchover occurs Flag must be cleared to clear interrupt	
2	BLF	0[2)]	Battery status ok	
		1	Battery status low; flag is read-only	
1	BSIE	0[2)]	No interrupt generated from battery switchover flag BSF	
		1	Interrupt generated when BSF is set	
0	BLIE	0[2)]	No interrupt generated from battery low flag BLF	
		1	Interrupt generated when BLF is set	

[1)] Default value is 111.
[2)] Default value.

8.3. TIME AND DATE REGISTERS

Most of these registers are coded in the Binary Coded Decimal (BCD) format. BCD is used to simplify application use. An example is shown for the array SECONDS.

8.3.1.SECONDS (address 03h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
03h	Seconds	OS	40	20	10	8	4	2	1

Bit	Symbol	Value	Description
7	OS	0	Clock integrity is guaranteed
		1[1)]	Clock integrity is not guaranteed Oscillator has stopped or been interrupted
6 to 0	Seconds	0 to 59	This register holds the current seconds coded in BCD format

[1)] Startup value.

Seconds value is decimal	Upper-digit (ten's place)			Digit (unit place)			
	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	0	0	0	0	0	0	0
01	0	0	0	0	0	0	1
02	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:
09	0	0	0	1	0	0	1
10	0	0	1	0	0	0	0
:	:	:	:	:	:	:	:
58	1	0	1	1	0	0	0
59	1	0	1	1	0	0	1

8.3.2.MINUTES (address 04h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04h	Minutes	X	40	20	10	8	4	2	1

Bit	Symbol	Value	Description
7	X	-	Unused
6 to 0	Minutes	0 to 59	This register holds the current minutes coded in BCD format

8.3.3.HOURS (address 05h…bits description)

12 hour mode[1)]

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
05h	Hours	X	X	AMPM	10	8	4	2	1

Bit	Symbol	Value	Description
7 to 6	X	-	Unused
5	AMPM	0	Indicates AM
		1	Indicates PM
4 to 0	Hours	1 to 12	This register holds the current hours in 12 hour mode coded in BCD format

[1)] Hour mode is set by bit 12_24 in register Control 1.

24 hour mode[1)]

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
05h	Hours	X	X	20	10	8	4	2	1

Bit	Symbol	Value	Description
7 to 6	X	-	Unused
5 to 0	Hours	0 to 23	This register holds the current hours in 24 hour mode coded in BCD format

[1)] Hour mode is set by bit 12_24 in register Control 1.

8.3.4.DAYS (address 06h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06h	Days	X	X	20	10	8	4	2	1

Bit	Symbol	Value	Description
7 to 6	X	-	Unused
5 to 0	Days[1)]	1 to 31	This register holds the current day coded in BCD format

[1)] If the year counter contains a value which is exactly divisible by 4 (including the year 00), the RV-8523 compensates for leap years by adding a 29th day to February.

8.3.5.WEEKDAYS (address 07h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
07h	Weekdays	X	X	X	X	X	4	2	1

Bit	Symbol	Value	Description
7 to 3	X	-	Unused
2 to 0	Weekdays	0 to 6	This register holds the current weekday

Weekdays[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sunday	X	X	X	X	X	0	0	0
Monday	X	X	X	X	X	0	0	1
Tuesday	X	X	X	X	X	0	1	0
Wednesday	X	X	X	X	X	0	1	1
Thursday	X	X	X	X	X	1	0	0
Friday	X	X	X	X	X	1	0	1
Saturday	X	X	X	X	X	1	1	0

[1)] Definition may be re-assigned by the user.

8.3.6.MONTHS (address 08h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h	Months	X	X	X	10	8	4	2	1

Bit	Symbol	Value	Description
7 to 5	X	-	Unused
4 to 0	Months	1 to 12	This register holds the current month coded in BCD format

Months	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	X	X	X	0	0	0	0	1
February	X	X	X	0	0	0	1	0
March	X	X	X	0	0	0	1	1
April	X	X	X	0	0	1	0	0
May	X	X	X	0	0	1	0	1
June	X	X	X	0	0	1	1	0
July	X	X	X	0	0	1	1	1
August	X	X	X	0	1	0	0	0
September	X	X	X	0	1	0	0	1
October	X	X	X	1	0	0	0	0
November	X	X	X	1	0	0	0	1
December	X	X	X	1	0	0	1	0

8.3.7. YEARS (address 09h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
09h	Years	80	40	20	10	8	4	2	1

Bit	Symbol	Value	Description
7 to 0	Years	0 to 99	This register holds the current year coded in BCD format

8.4. ALARM REGISTERS

The registers at addresses 0Ah through 0Dh contain the alarm information.

8.4.1. MINUTE ALARM (address 0Ah…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Ah	Minute Alarm	AE_M	40	20	10	8	4	2	1

Bit	Symbol	Value	Description
7	AE_M	0	Minute Alarm in enabled
		1[1)]	Minute Alarm is disabled
6 to 0	Minute Alarm	0 to 59	Minute Alarm information coded in BCD format

[1)] Default value.

8.4.2. HOUR ALARM (address 0Bh…bits description)

12 hour mode[1)]

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Bh	Hour Alarm	AE_H	X	AMPM	10	8	4	2	1

Bit	Symbol	Value	Description
7	AE_H	0	Hour Alarm in enabled
		1[2)]	Hour Alarm is disabled
6	X	-	Unused
5	AMPM	0	Indicates AM
		1	Indicates PM
4 to 0	Hour Alarm	1 to 12	Hour Alarm information in 12 hour mode coded in BCD format

[1)] Hour mode is set by bit 12_24 in register Control 1.
[2)] Default value.

24 hour mode[1)]

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Bh	Hour Alarm	AE_H	X	20	10	8	4	2	1

Bit	Symbol	Value	Description
7	AE_H	0	Hour Alarm in enabled
		1[2)]	Hour Alarm is disabled
6	X	-	Unused
5 to 0	Hour Alarm	0 to 23	Hour Alarm information in 24 hour mode coded in BCD format

[1)] Hour mode is set by bit 12_24 in register Control 1.
[2)] Default value.

8.4.3.DAY ALARM (address 0Ch…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Ch	Day Alarm	AE_D	X	20	10	8	4	2	1

Bit	Symbol	Value	Description
7	AE_D	0	Day Alarm in enabled
		1[1)]	Day Alarm is disabled
6	X	-	Unused
5 to 0	Day Alarm	1 to 31	Day Alarm information coded in BCD format

[1)] Default value.

8.4.4.WEEKDAY ALARM (address 0Dh…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Dh	Weekday Alarm	AE_W	X	X	X	X	4	2	1

Bit	Symbol	Value	Description
7	AE_W	0	Weekday Alarm in enabled
		1[1)]	Weekday Alarm is disabled
6 to 3	X	-	Unused
2 to 0	Weekday Alarm	0 to 6	Weekday Alarm information

[1)] Default value.

8.5. FREQUENCY OFFSET REGISTER

The RV-8523 incorporates an offset register (address 0Eh), which can be used to implement several functions, like:

- Aging adjustment
- Temperature compensation
- Accuracy tuning

8.5.1.FREQUENCY OFFSET (address 0Eh…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Eh	Frequency Offset	MODE	Offset value						

Bit	Symbol	Value	Description
7	MODE	0[1)]	Offset is made once every two hours
		1	Offset is made once every minute
6 to 0	Offset	+63/-64	Offset value (see table below)

[1)] Default value.

For MODE = 0, each LSB introduces an offset of 4.34 ppm. For MODE = 1, each LSB introduces an offset of 4.069 ppm. The values of 4.34 ppm and 4.069 ppm are based on a nominal 32.768 kHz clock. The offset value is coded in two's complement giving a range of +63 LSB to -64 LSB.

Offset [6:0]	Offset value in decimal	Offset value in ppm	
		Every two hours (MODE = 0)	Every minute (MODE = 1)
0111111	+63	+273.420	+256.347
0111110	+62	+269.080	+252.278
:	:	:	:
0000010	+2	+8.680	+8.138
0000001	+1	+4.340	+4.069
0000000	0[1)]	0[1)]	0[1)]
1111111	-1	-4.340	-4.069
1111110	-2	-8.680	-8.138
:	:	:	:
1000001	-63	-273.420	-256.347
1000000	-64	-277.760	-260.416

[1)] Default value.

The correction is made by adding or subtracting clock correction pulses, thereby changing the period of a single second.

It is possible to monitor when correction pulses are applied. To enable correction interrupt generation, bit CIE (register Control 1) has to be set logic 1. At every correction cycle a $^1/_{4096}$ s pulse is generated on pin $\overline{\text{INT\_x}}$. If multiple correction pulses are applied, a $^1/_{4096}$ s interrupt pulse is generated for each correction pulse applied.

8.6. TIMER AND CLKOUT REGISTERS

The RV-8523 has three timers:

- Timer A can be used as a watchdog timer or a countdown timer (see section 9.9.1.). It can be configured by using TAC [1:0] in the Timer & CLKOUT register (0Fh)
- Timer B can be used as a countdown timer (see section 9.9.2.). It can be configured by using TBC in the Timer & CLKOUT register (0Fh)
- Second interrupt timer is used to generate an interrupt once per second (see section 9.9.3.)

Timer A and timer B both have five selectable source clocks allowing for countdown periods from less than 1 ms to 255 h. To control the timer functions and timer output, the registers 01h, 0Fh, 10h, 11h, 12h and 13h are used.

8.6.1.TIMER & CLKOUT (address 0Fh…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Fh	Timer & CLKOUT	TAM	TBM	COF2	COF1	COF0	TAC1	TAC0	TBC

Bit	Symbol	Value	Description
7	TAM	0[1)]	Permanent active interrupt for timer A and for the second interrupt timer
		1	Pulsed interrupt for timer A and the second interrupt timer
6	TBM	0[1)]	Permanent active interrupt for timer B
		1	Pulsed interrupt for timer B
5 to 3	COF[2:0]	000[1)] to 111	CLKOUT frequency selection (see section 9.8.)
2 to 1	TAC[1:0]	00[1)] or 11	Timer A is disabled
		01	Timer A is configures as countdown timer If CTAIE (register Control 2) is set logic 1, the interrupt is activated when the countdown timed out
		10	Timer A is configured as watchdog timer If WTAIE (register Control 2) is set logic 1, the interrupt is activated when timed out
0	TBC	0[1)]	Timer B is disabled
		1	Timer B is enabled If CTBIE (register Control 2) is set logic 1, the interrupt is activated when the countdown timed out

[1)] Default value.

8.6.2.TIMER A CLOCK (address 10h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10h	Timer A Clock	X	X	X	X	X	TAQ2	TAQ1	TAQ0

Bit	Symbol	Value	Description
7 to 3	X	-	Unused
2 to 0	TAQ[2:0][1)]	000	4.096 kHz
		001	64 Hz
		010	1 Hz
		011	$^1/_{60}$ Hz
		111[2)] 110 100	$^1/_{3600}$ Hz

[1)] Source clock for timer A (see section 9.9.).
[2)] Default value.

8.6.3.TIMER A (address 11h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
11h	Timer A	128	64	32	16	8	4	2	1

Bit	Symbol	Value	Description
7 to 0	Timer A	00 to FF	Timer period in seconds Countdown value = n $\text{Timer Period} = \frac{n}{\text{Source Clock Frequency}}$

8.6.4.TIMER B CLOCK (address 12h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12h	Timer B Clock	X	TBW2	TBW1	TBW0	X	TBQ2	TBQ1	TBQ0

Bit	Symbol	Value	Description
7	X	-	Unused
6 to 4	TBW[2:0][2)]	000[1)]	46.875 ms
		001	62.500 ms
		010	78.125 ms
		011	93.750 ms
		100	125.000 ms
		101	156.250 ms
		110	187.500 ms
		111	218.750 ms
3	X	-	Unused
2 to 0	TBQ[2:0][3)]	000	4.096 kHz
		001	64 Hz
		010	1 Hz
		011	$^1/_{60}$ Hz
		111[1)] 110 100	$^1/_{3600}$ Hz

[1)] Default value.
[2)] Low pulse width for pulsed timer B interrupt.
[3)] Source clock for timer B (see section 9.9.)

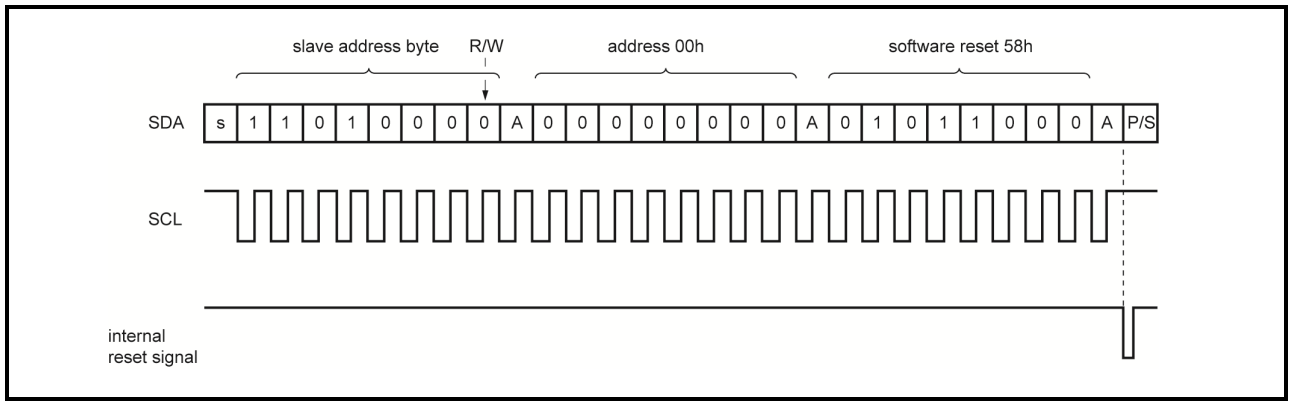
8.6.5.TIMER B (address 13h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
13h	Timer B	128	64	32	16	8	4	2	1

Bit	Symbol	Value	Description
7 to 0	Timer B	00 to FF	Timer period in seconds Countdown value = n $\text{Timer Period} = \frac{n}{\text{Source Clock Frequency}}$

8.7. RESET

A reset is automatically generated at power-on. A reset can also be initiated with the software reset command. Software reset command means setting bits 6, 4 and 3 in register Control 1 (00h) logic 1 and all others bits logic 0 by sending the bits sequence 01011000 (58h), see figure below.



After reset, the following mode is entered:

- 32.768 kHz CLKOUT active
- 24 hour mode is selected
- Register Frequency Offset is set logic 0
- No alarm set
- Timers disabled
- No interrupts enabled
- Battery switchover is disabled
- Battery low detection is disabled

8.7.1. REGISTER RESET VALUES

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	Control 1	0	0	0	0	0	0	0	0
01h	Control 2	0	0	0	0	0	0	0	0
02h	Control 3	1	1	1	X	0	0	0	0
03h	Seconds	1	-	-	-	-	-	-	-
04h	Minutes	X	-	-	-	-	-	-	-
05h	Hours	X	X	-	-	-	-	-	-
06h	Days	X	X	-	-	-	-	-	-
07h	Weekdays	X	X	X	X	X	-	-	-
08h	Months	X	X	X	-	-	-	-	-
09h	Years	-	-	-	-	-	-	-	-
0Ah	Minute Alarm	1	-	-	-	-	-	-	-
0Bh	Hour Alarm	1	X	-	-	-	-	-	-
0Ch	Day Alarm	1	X	-	-	-	-	-	-
0Dh	Weekday Alarm	1	X	X	X	X	-	-	-
0Eh	Frequency Offset	0	0	0	0	0	0	0	0
0Fh	Timer & CLKOUT	0	0	0	0	0	0	0	0
10h	Timer A Clock	X	X	X	X	X	1	1	1
11h	Timer A	-	-	-	-	-	-	-	-
12h	Timer B Clock	X	0	0	0	X	1	1	1
13h	Timer B	-	-	-	-	-	-	-	-

Bit positions labeled as “-” are undefined at power-on and unchanged by subsequent resets.
Bit positions labeled as “X” are not implemented and will return 0 when read.

9. DETAILED FUNCTIONAL DESCRIPTION

9.1. INTERRUPT

Active low interrupt signals are available at pin $\overline{\text{INT\_1}}$/CLKOUT and $\overline{\text{INT\_2}}$. Pin $\overline{\text{INT\_1}}$/CLKOUT has both functions of $\overline{\text{INT\_1}}$ and CLKOUT combined.

$\overline{\text{INT\_1}}$ Interrupt output may be sourced from different places:

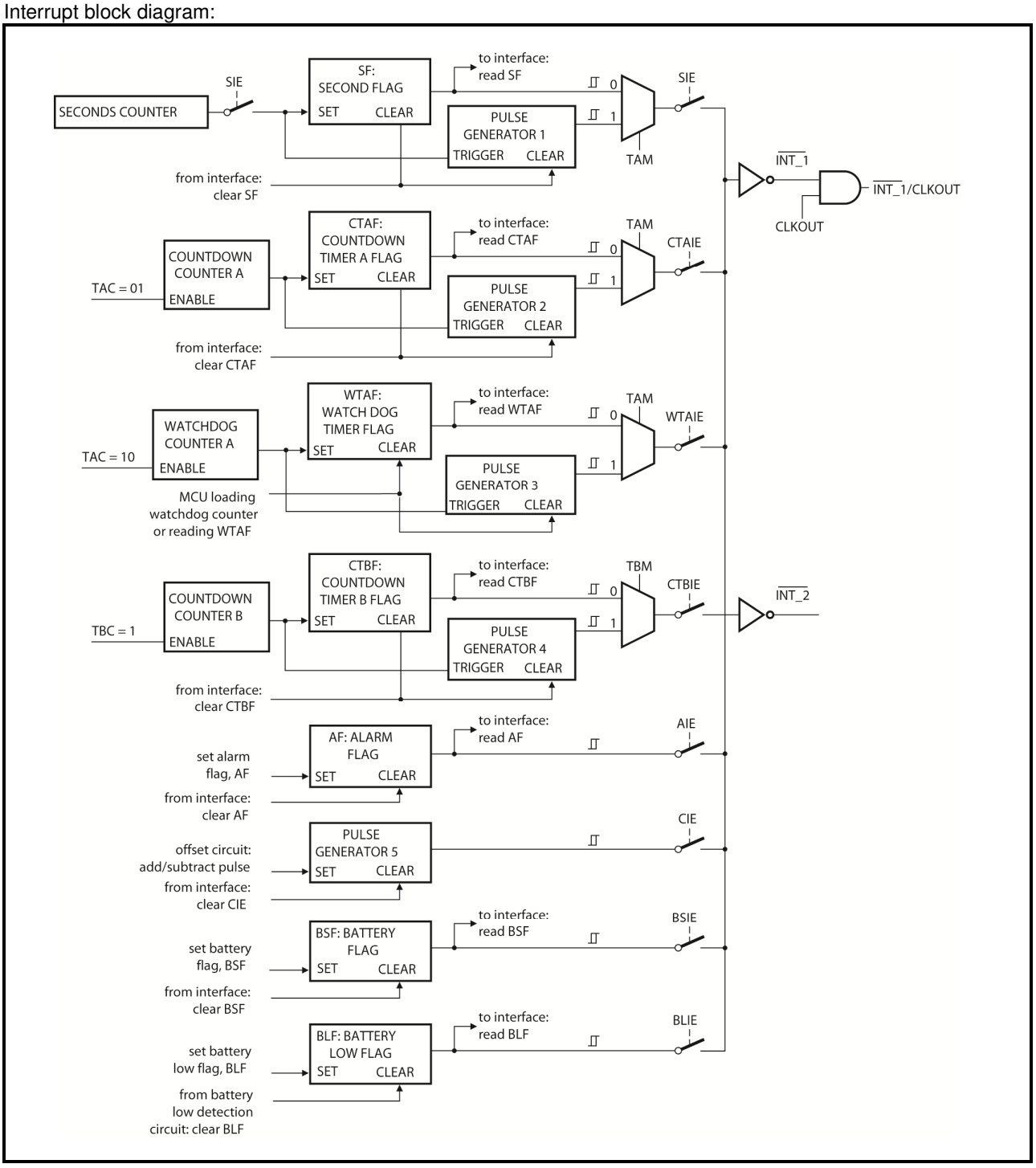
- Second timer
- Timer A
- Timer B
- Alarm
- Battery switchover
- Battery low detection
- Clock offset correction pulse

$\overline{\text{INT\_2}}$ interrupt output is sourced only from timer B.

The control bit TAM (register Timer & CLKOUT) is used to configure whether the interrupts generated from the second interrupt timer and timer A are pulsed signals or a permanently active signal. The control bit TBM (register Timer & CLKOUT) is used to configure whether the interrupt generated from timer B is a pulsed signal or a permanently active signal. All the other interrupt sources generate a permanently active interrupt signal, which follows the status of the corresponding flags.

- The flags SF, CTAF, CTBF, AF and BSF can be cleared by using the interface
- WTAF is read only. A read of the register Control 2 (01h) will automatically resets WTAF (WTAF = 0) and clear the interrupt
- The flag BLF is read only. It is cleared automatically from the battery low detection circuit when the battery is replaced

Interrupt block diagram:



Note:

When SIE, CTAIE, WTAIE, CTBIE, AIE, CIE, BSIE, BLIE and clock-out are disabled, then $\overline{INT\_1}$ will remains high-impedance. When CTBIE is disabled, then $\overline{INT\_2}$ will remain high-impedance.

9.2. POWER MANAGEMENT

The RV-8523 has two power supply pins:

- V_{DD} - the main power supply input pin
- V_{BAT} - the battery backup input pin

The RV-8523 has two power management functions implemented:

- Battery switchover function
- Battery low detection function

The power management functions are controlled by the control bits PM[2:0] in register Control 3 (02h):

PM[2:0]	Function
000	Battery switchover function is enabled in standard mode Battery low detection function is enabled
001	Battery switchover function is enabled in direct switching mode Battery low detection function is enabled
010, 011[1)]	Battery switchover function is disabled - only one power supply (V_{DD}) Battery low detection function is enabled
100	Battery switchover function is enabled in standard mode Battery low detection function is disabled
101	Battery switchover function is enabled in direct switching mode Battery low detection function is disabled
110	Not allowed
111[2) 3)]	Battery switchover function is disabled - only one power supply (V_{DD}) Battery low detection function is disabled

[1)] When the battery switchover function is disabled, the RV-8523 works only with the power supply V_{DD}.
[2)] When the battery switchover function is disabled, the RV-8523 works only with the power supply V_{DD}; V_{BAT} must be put to ground and the battery low detection function is disabled.
[3)] Default value.

9.2.1.STANDBY MODE

When the device is first powered up from the battery (V_{BAT}) but without a main supply (V_{DD}), the RV-8523 automatically enters the standby mode. In standby mode the RV-8523 does not draw any power from the backup battery until the device is powered up from the main power supply V_{DD}. Thereafter, the device switches over to battery backup mode whenever the main power supply V_{DD} is lost.

It is also possible to enter into standby mode when the chip is already supplied by the main power supply V_{DD} and a backup battery is connected. To enter the standby mode, the power management control bits PM[2:0] have to be set logic 111. Then the main power supply V_{DD} must be removed. As a result of it, the RV-8523 enters the standby mode and does not draw any current from the backup battery before it is powered up again from main supply V_{DD}.

9.2.2.BATTERY SWITCHOVER

The RV-8523 has a backup battery switchover circuit. It monitors the main power supply V_{DD} and switches automatically to the backup battery when a power failure condition is detected.

One of two operation modes can be selected:

- **Standard mode:** the power failure condition happens when: $V_{DD} < V_{BAT}$ AND $V_{DD} < V_{th(sw)bat}$
- **Direct switching mode:** the power failure condition happens when $V_{DD} < V_{BAT}$.
  Direct switching from V_{DD} to V_{BAT} without requiring V_{DD} to drop below $V_{th(sw)bat}$

$V_{th(sw)bat}$ is the battery switch threshold voltage. Typical value is 2.5 V.

Generation of interrupts from the battery switchover is controlled via the BSIE bit (register Control 2). If BSIE is enabled, the $\overline{INT\_1}$ follows the status of bit BLF (register Control 3). Clearing BLF immediately clears $\overline{INT\_1}$.

When a power failure condition occurs and the power supply switches to the battery, the following sequence occurs:

1. The battery switch flag BSF (register Control 3) is set logic 1
2. An interrupt is generated if the control bit BSIE (register Control 3) is enabled

The battery switch flag BSF can be cleared by using the interface after the power supply has switched to V_{DD}. It must be cleared to clear the interrupt.

The interface is disabled in battery backup operation:

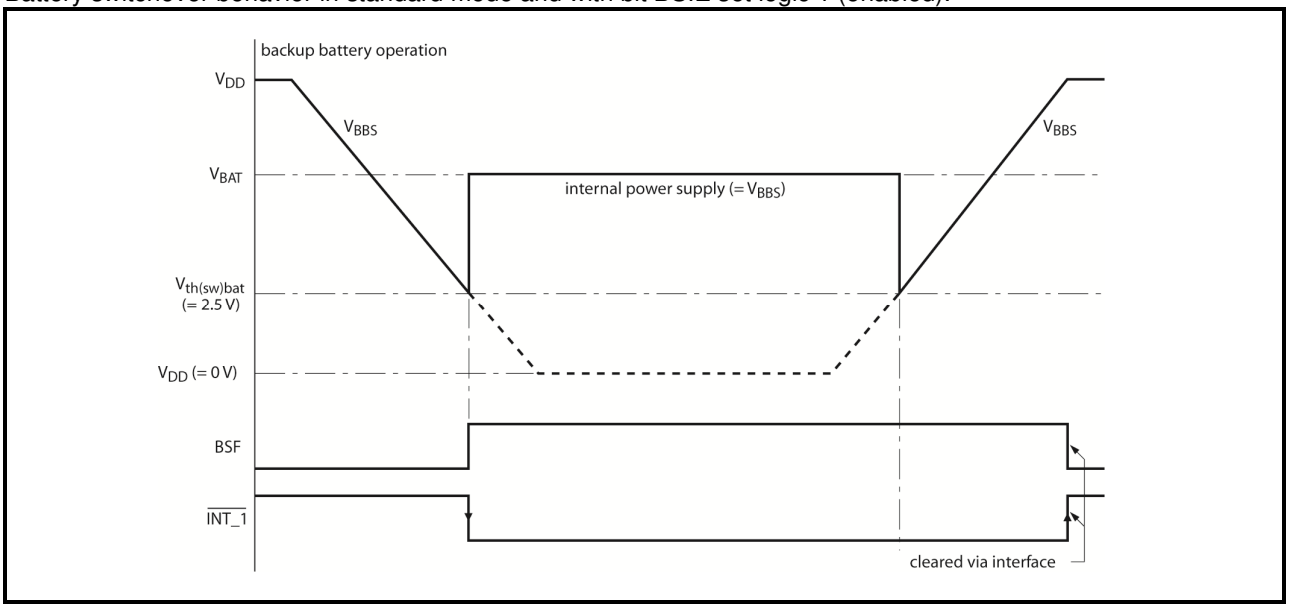
- Interface inputs are not recognized, preventing extraneous data being written to the device
- Interface outputs are high-impedance

Standard mode:

If $V_{DD} > V_{BAT}$ OR $V_{DD} > V_{th(sw)bat}$ the internal power supply is V_{DD}.

If $V_{DD} < V_{BAT}$ AND $V_{DD} < V_{th(sw)bat}$ the internal power supply is V_{BAT}.

Battery switchover behavior in standard mode and with bit BSIE set logic 1 (enabled):



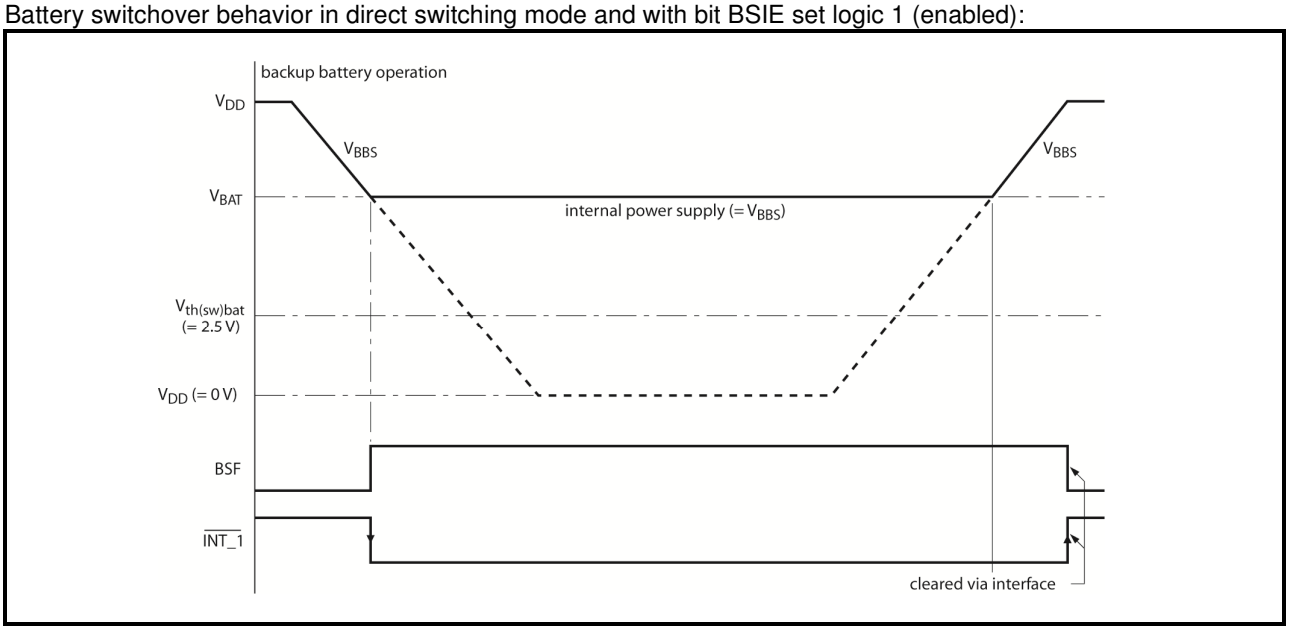
Direct switching mode:

If $V_{DD} > V_{BAT}$ the internal power supply is V_{DD}.

If $V_{DD} < V_{BAT}$ the internal power supply is V_{BAT}.

The direct switching mode is useful in systems where V_{DD} is higher than V_{BAT} at all times (for example V_{DD} = 5 V, V_{BAT} = 3.5 V). If V_{DD} and V_{BAT} values are similar (for example V_{DD} = 3.3 V, $V_{BAT} \geq$ 3.0 V), the direct switching mode is not recommended. In direct switching mode, the power consumption is reduced compared to the standard mode because the monitoring of V_{DD} and $V_{th(sw)bat}$ is not performed.

Battery switchover behavior in direct switching mode and with bit BSIE set logic 1 (enabled):



Battery switchover disabled, only one power supply (V_{DD}):

When the battery switchover function is disabled:

- The power supply is applied on V_{DD} pin
- V_{BAT} pin must be connected to ground
- The battery flag (BSF) is always logic 0

9.2.3.BATTERY LOW DETECTION

The RV-8523 has a battery low detection circuit, which monitors the status of the battery V_{BAT}.

Generation of interrupts from the battery low detection is controlled via bit BLIE (register Control 3). If BLIE is enabled, the $\overline{INT\_1}$ follows the status of bit BLF (register Control 3).

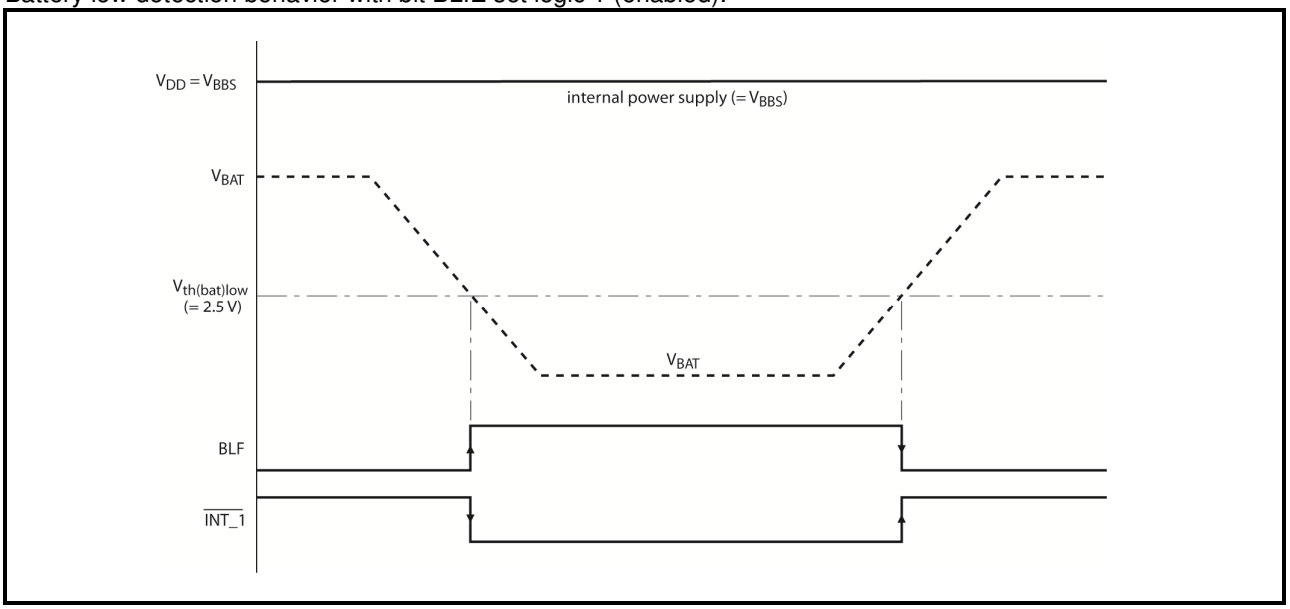
When V_{BAT} drops below the threshold value $V_{th(bat)low}$ (typically 2.5 V), the BLF flag (register Control 3) is set to indicate that the battery is low and that it must be replaced. Monitoring of the battery voltage also occurs during battery operation.

An unreliable battery does not ensure data integrity during periods of backup battery operation.

When V_{BAT} drops below the threshold value $V_{th(bat)low}$, the following sequence occurs:

1. The battery low flag BLF is set logic 1
2. An interrupt is generated if the control bit BLIE (register Control 3) is enabled. The interrupt remains active until the battery is replaced (BLF set logic 0) or when bit BLIE is disabled (BLIE set logic 0)
3. The flag BLF (register Control 3) remains logic 1 until the battery is replaced. BLF cannot be cleared using the interface. It is cleared automatically by the battery low detection circuit when the battery is replaced

Battery low detection behavior with bit BLIE set logic 1 (enabled):

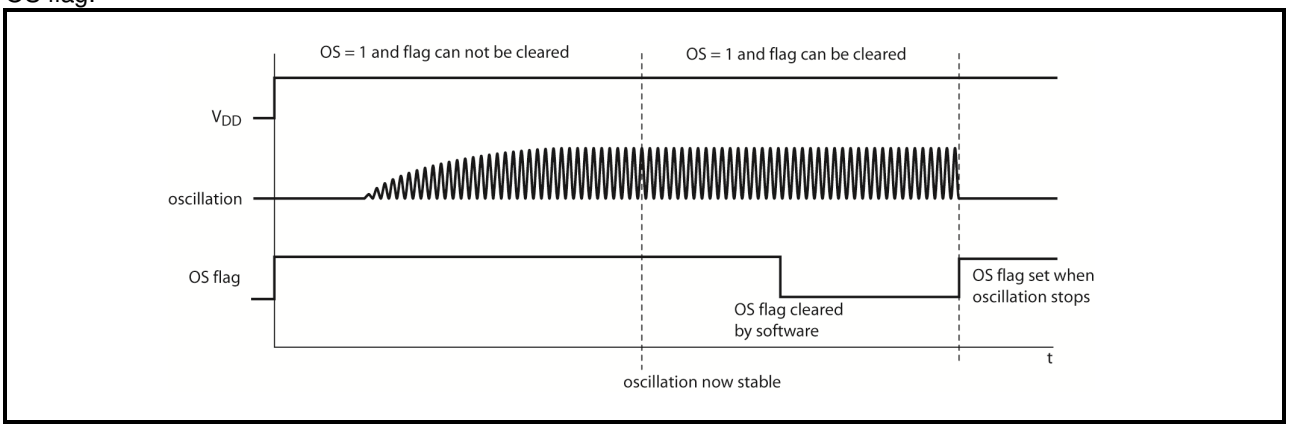


9.3. OSCILLATOR STOP FLAG

The OS flag is set whenever the oscillator is stopped. The flag remains set until cleared by using the interface. When the oscillator is not running, then the OS flag cannot be cleared. This method can be used to monitor the oscillator.

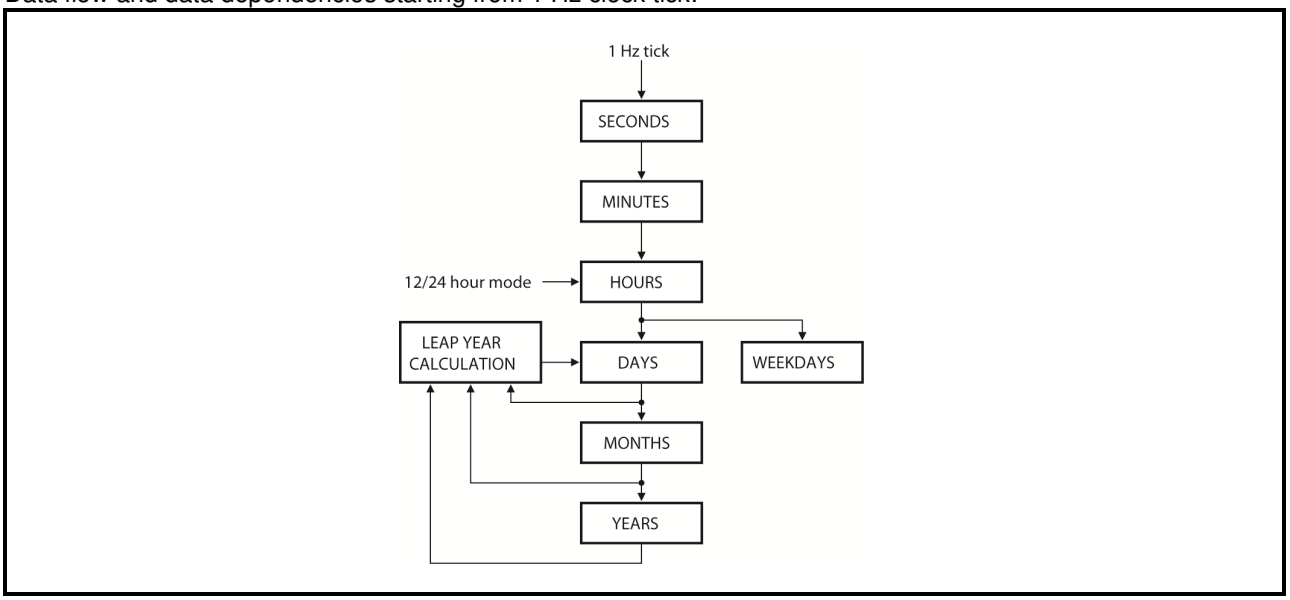
The oscillator is considered to be stopped during the time between power-on and stable crystal resonance. This time may be in a range of 200 ms to 2 s, depending on temperature and supply voltage. At power-on, the OS flag is always set.

OS flag:



9.4. DATA FLOW ON THE TIME FUNCTION

Data flow and data dependencies starting from 1 Hz clock tick:



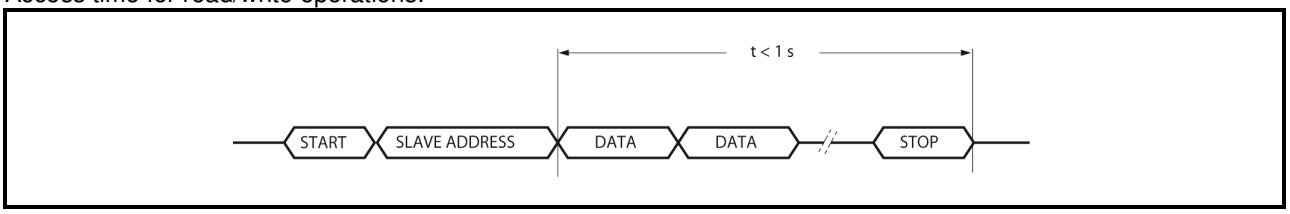
During read/write operations, the time counting circuits (memory locations 03h through 09h) are blocked.

The blocking prevents:

- Faulty reading of the clock and calendar during a carry condition
- Incrementing the time registers during the read cycle

After the read/write access is completed, the time circuit is released again and any pending request to increment the time counters that occurred during the read/write access is serviced. A maximum of one request can be stored; therefore, all accesses must be completed within 1 second.

Access time for read/write operations:



Because of this method, it is very important to make a read or write access in one go, that is, setting or reading seconds through years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

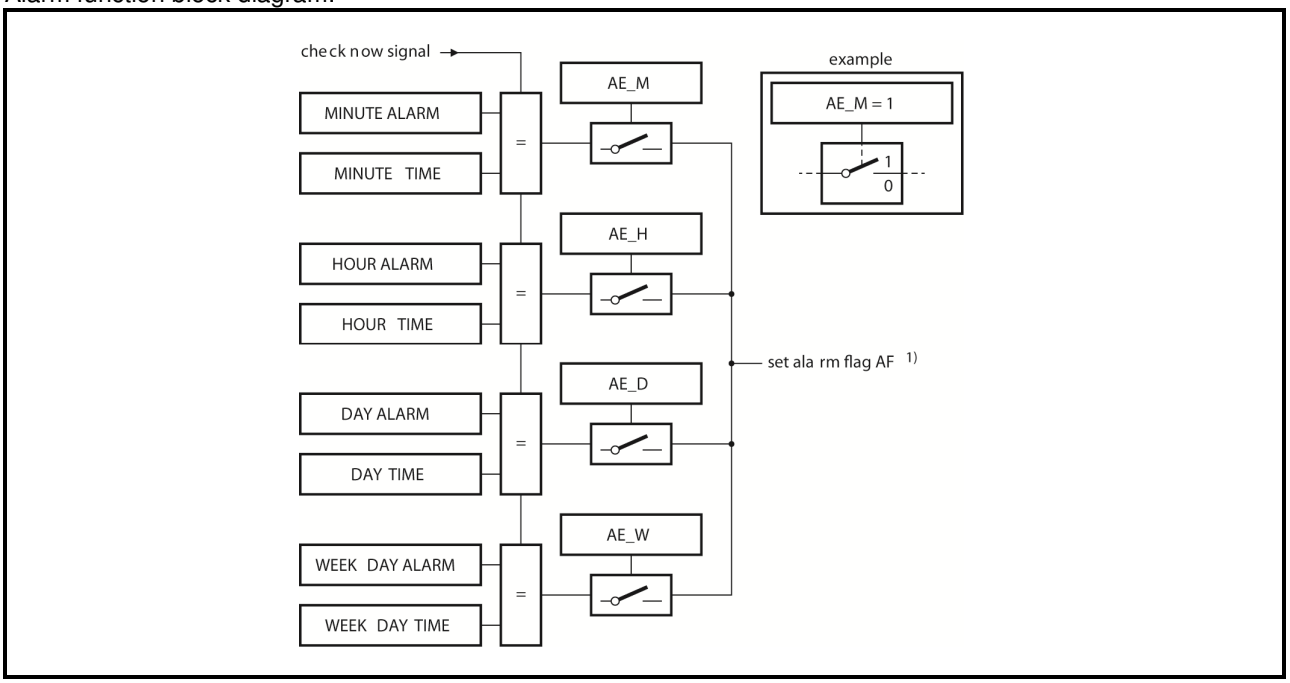
As an example, if the time (seconds through hours) is set in one access and then in a second access the date is set, it is possible that the time will increment between the two accesses. A similar problem exists when reading. A rollover may occur between reads thus giving the minutes from one moment and the hours from the next.

Recommended method for reading the time:

1. Send a START condition and the slave address for write (D0h)
2. Set the address pointer to 3 (Seconds) by sending 03h
3. Send a RE-START condition (STOP followed by START)
4. Send the slave address for read (D1h)
5. Read the seconds
6. Read the minutes
7. Read the hours
8. Read the days
9. Read the weekdays
10. Read the months
11. Read the years
12. Send a STOP condition

9.5. ALARM FLAG

Alarm function block diagram:



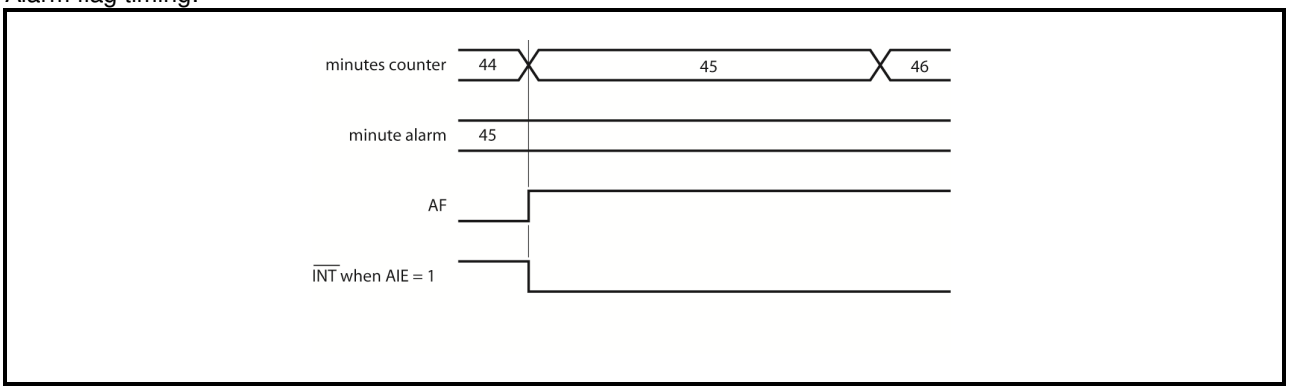
1) Only when all enabled alarm settings are matching. It's only on increment to a matched case that the alarm flag is set.

When one or several alarm registers are loaded with a valid minute, hour, day, or weekday value and its corresponding alarm enable bit (AE_x) is logic 0, then that information is compared with the current minute, hour, day, and weekday value. When all enabled comparisons first match, the alarm flag, AF (register Control 2), is set logic 1.

The generation of interrupts from the alarm function is controlled via bit AIE (register Control 1). If bit AIE is enabled, then the $\overline{INT}$_1 pin follows the condition of bit AF. AF remains set until cleared by the interface. Once AF has been cleared, it will only be set again when the time increments to match the alarm condition once more. Alarm registers, which have their AE_x bit logic 1 are ignored. The generation of interrupts from the alarm function is described more detailed in section 9.1.

Next page tables show an example for clearing bit AF. Clearing the flag is made by a write command, therefore bits 2, 1, and 0 must be re-written with their previous values. Repeatedly re-writing these bits has no influence on the functional behavior.

Alarm flag timing:



To prevent the timer flags being overwritten while clearing bit AF, logic AND is performed during a write access. A flag is cleared by writing logic 0 while a flag is not cleared by writing logic 1. Writing logic 1 results in the flag value remaining unchanged.

Flag location in register Control 2:

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01h	Control 2	WTAF	CTAF	CTBF	SF	AF	-	-	-

The table below shows what instruction must be sent to clear bit AF. In this example, bit CTAF, CTBF and bit SF are unaffected.

Example to clear only AF (bit 3):

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01h	Control 2	0	1	1	1	0	-	-	-

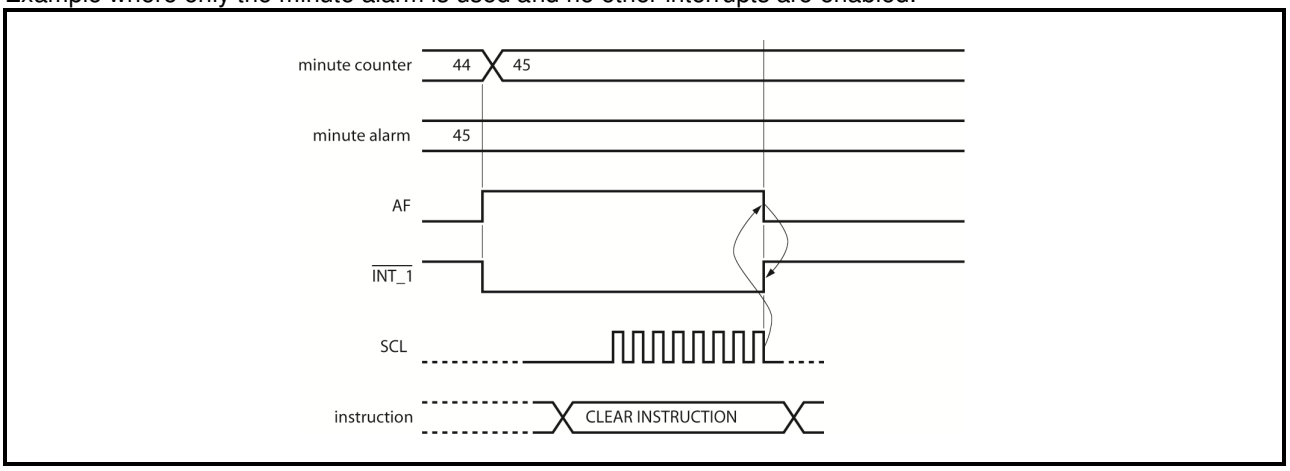
Note:

The bits labeled as "-" have to be re-written with the previous values.

9.6. ALARM INTERRUPTS

Generation of interrupts from the alarm function is controlled via the bit AIE (register Control 1). If AIE is enabled, the $\overline{\text{INT\_1}}$ follows the status of bit AF (register Control 2). Clearing AF immediately clears $\overline{\text{INT\_1}}$. No pulse generation is possible for alarm interrupts.

Example where only the minute alarm is used and no other interrupts are enabled:



9.7. OFFSET

9.7.1.CORRECTION WHEN MODE = 0

The correction is triggered once per two hours and then correction pulses are applied once per minute until the programmed correction values have been implemented.

Correction pulses for MODE = 0:

Correction value	Hour	Minute	Correction pulses on $\overline{INT\_1}$ per minute[1)]
+1 or -1	02	00	1
+2 or -2	02	00 and 01	1
+3 or -3	02	00, 01 and 02	1
:	:	:	:
+59 or -59	02	00 to 58	1
+60 or -60	02	00 to 59	1
+61 or -61	02 03	00 to 59 00	1 1
+62 or -62	02 03	00 to 59 00 and 01	1 1
+63 or -63	02 03	00 to 59 00, 01 and 02	1 1
-64	02 03	00 to 59 00, 01, 02 and 03	1 1

[1)] The correction pulses on pin $\overline{INT\_1}$ are $^1/_{64}$ s wide.

In MODE = 0, any timer or clock output using a frequency below 64 Hz is affected by the clock correction.

Effect of clock correction for MODE = 0:

CLKOUT frequency (Hz)	Effect of correction	Timer source clock frequency (Hz)	Effect of correction
32'768	No effect	4'096	No effect
16'384	No effect	64	No effect
8'192	No effect	1	Affected
4'096	No effect	$^1/_{60}$	Affected
1'024	No effect	$^1/_{3600}$	Affected
32	Affected	-	-
1	Affected	-	-

9.7.2.CORRECTION WHEN MODE = 1

The correction is triggered once per minute and then correction pulses are applied once per second up to a maximum of 60 pulses. When correction values greater than 60 pulses are used, additional correction pulses are made in the 59th second.

Clock correction is made more frequently in MODE = 1; however, this can result in higher power consumption.

Correction pulses for MODE = 1:

Correction value	**Minute**	**Second**	**Correction pulses on $\overline{INT\_1}$ per second[1)]**
+1 or -1	02	00	1
+2 or -2	02	00 and 01	1
+3 or -3	02	00, 01 and 02	1
:	:	:	:
+59 or -59	02	00 to 58	1
+60 or -60	02	00 to 59	1
+61 or -61	02 02	00 to 58 59	1 2
+62 or -62	02 02	00 to 58 59	1 2
+63 or -63	02 02	00 to 58 59	1 4
-64	02 02	00 to 58 59	1 5

[1)] The correction pulses on pin $\overline{INT\_x}$ are $^1/_{4096}$ s wide. For multiple pulses, they are repeated at an interval of $^1/_{2048}$ s.

In MODE = 1, any timer source clock output using a frequency below 4.096 kHz is also affected by the clock correction.

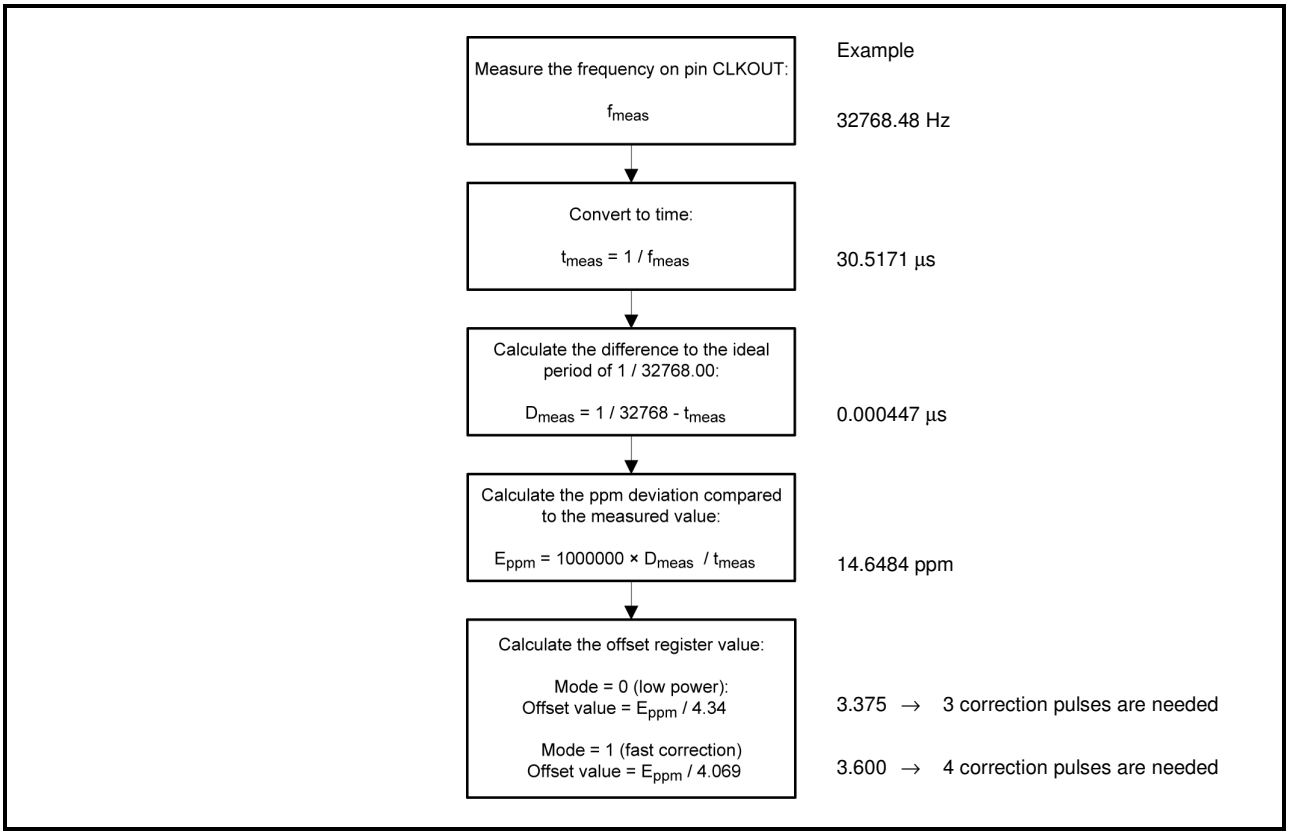
Effect of clock correction for MODE = 1:

CLKOUT frequency (Hz)	**Effect of correction**	**Timer source clock frequency (Hz)**	**Effect of correction**
32’768	No effect	4’096	No effect
16’384	No effect	64	Affected
8’192	No effect	1	Affected
4’096	No effect	$^1/_{60}$	Affected
1’024	No effect	$^1/_{3600}$	Affected
32	Affected	-	-
1	Affected	-	-

9.7.3.OFFSET CALIBRATION WORKFLOW

The calibration offset has to be calculated based on the time. The figure below shows the workflow how the offset register values can be calculated:

Offset calibration calculation workflow:



9.8. CLKOUT FREQUENCY SELECTION

Clock output operation is controlled by the COF[2:0] in the Timer & CLKOUT register. Frequencies of 32.768 kHz (default) down to 1 Hz can be generated (see table below) for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator.

A programmable square wave is available at pin $\overline{INT\_1}$ and pin CLKOUT, which are both open-drain outputs. Pin $\overline{INT\_1}$ has both functions of $\overline{INT\_1}$ and CLKOUT combined.

The duty cycle of the selected clock is not controlled but due to the nature of the clock generation, all clock frequencies except 32.768 kHz have a duty cycle of 50 : 50.

The STOP bit function can also affect the CLKOUT signal, depending on the selected frequency. When STOP is active, the $\overline{INT\_1}$ and CLKOUT pins will be high-impedance for all frequencies except of 32.768 kHz, 16.384 kHz and 8.192 kHz. For more details, see section 9.10.

COF[2:0]	CLKOUT frequency (Hz)	Typical duty cycle[1)]	Effect of STOP bit
000[2)]	32'768	60 : 40 to 40 : 60	No effect
001	16'384	50 : 50	No effect
010	8'192	50 : 50	No effect
011	4'096	50 : 50	CLKOUT = high-Z
100	1'024	50 : 50	CLKOUT = high-Z
101	32	50 : 50[3)]	CLKOUT = high-Z
110	1	50 : 50[3)]	CLKOUT = high-Z
111	CLKOUT disabled (high-Z)		

[1)] Duty cycle definition: % HIGH-level time : % LOW-level time.
[2)] Default value.
[3)] Clock frequencies may be affected by offset correction.

9.9. TIMER

Programmable timer characteristics:

TAQ[2:0] TBQ[2:0]	Timer source clock frequency	Units	Minimum timer-period (n = 1)	Units	Maximum timer-period (n = 255)	Units
000	4.096	kHz	244	µs	62.256	ms
001	64	Hz	15.625	ms	3.984	s
010	1	Hz	1	s	255	s
011	$^1/_{60}$	Hz	1	min	255	min
111 110 100	$^1/_{3600}$	Hz	1	hour	255	hour

9.9.1.TIMER A

With the bit field TAC[1:0] in register Timer & CLKOUT (0Fh) Timer A can be configured as a countdown timer (TAC[1:0] = 01) or watchdog timer (TAC[1:0] = 10).

Watchdog timer function:

The three bits TAQ[2:0] in register Timer A Clock (10h) determine one of the five source clock frequencies for the watchdog timer: 4.096 kHz, 64 Hz, 1 Hz, $^1/_{60}$ Hz or $^1/_{3600}$ Hz (see section 8.6.2.).

The generation of interrupts from the watchdog timer is controlled by using WTAIE bit (register Control 2).

When configured as a watchdog timer (TAC[1:0] = 10), the 8-bit timer value in register Timer A (11h) determines the watchdog timer-period.

The watchdog timer counts down from value n in register Timer A (11h). When the counter reaches 1, the watchdog timer flag WTAF (register Control 2) is set logic 1 on the next rising edge of the timer clock (see figure below). In that case:

- If WTAIE = 1, an interrupt will be generated
- If WTAIE = 0, no interrupt will be generated

The interrupt generated by the watchdog timer function of timer A may be generated as pulsed signal or a permanently active signal. The TAM bit (register Timer & CLKOUT) is used to control the interrupt generation mode.

The counter does not automatically reload. When loading the counter with any valid value of n, except 0:

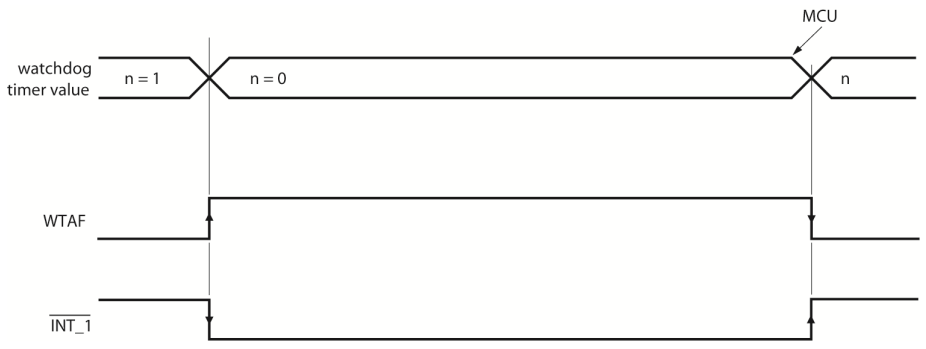
- The flag WTAF is reset (WTAF = 0)
- Interrupt is cleared
- The watchdog timer starts

When loading the counter with 0:

- The flag WTAF is reset (WTAF = 0)
- Interrupt is cleared
- The watchdog timer stops

WTAF is read only. A read of the register Control 2 (01h) automatically resets WTAF (WTAF = 0) and clears the interrupt.

Watchdog activates an interrupt when timed out:



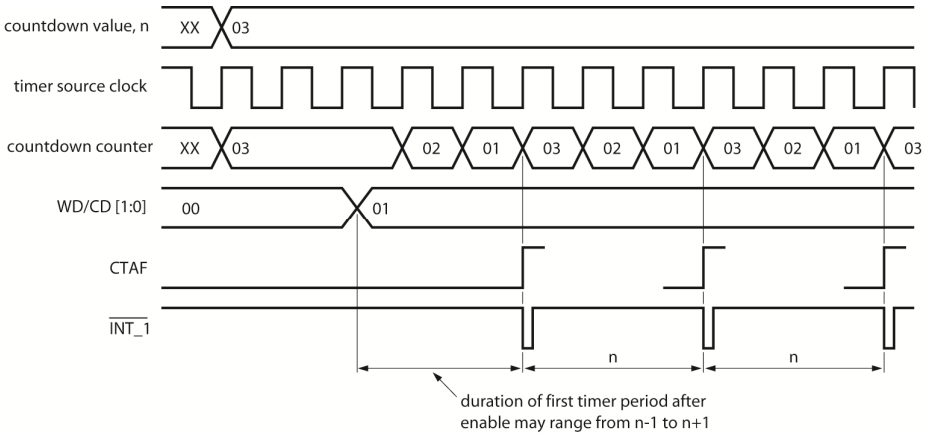
TAC[1:0] = 10, WTAIE = 1, WTAF = 1, an interrupt is generated.

Countdown timer function:

When configured as a countdown timer (TAC[1:0] = 01), timer A counts down from the software programmed 8-bit binary value n in register Timer A (11h). When the counter reaches 1, the following events occur on the next rising edge of the timer clock (see figure below):

- The countdown timer flag CTAF (register Control 2) is set logic 1
- When the interrupt generation is enabled (CTAIE = 1), an interrupt signal on $\overline{INT\_1}$ is generated
- The counter automatically reloads
- The next timer-period starts

General countdown timer behavior:



In this example, it is assumed that the countdown timer flag (CTAF) is cleared before the next countdown period expires and that the interrupt output is set to pulse mode.

At the end of every countdown, the timer sets the countdown timer flag CTAF (register Control 2). CTAF may only be cleared by using the interface. Instructions, how to clear a flag, are given in section 9.5.

When reading the timer, the current countdown value is returned and **not** the initial value n. Since it is not possible to freeze the countdown timer counter during read back, it is recommended to read the register twice and check for consistent results.

If a new value of n is written before the end of the actual timer-period, this value takes immediate effect. It is not recommended to change n without first disabling the counter by setting TAC[1:0] = 00 (register Timer & CLKOUT). The update of n is asynchronous to the timer clock. Therefore changing it on the fly could result in a corrupted value loaded into the countdown counter. This can result in an undetermined countdown period for the first period. The countdown value n will be correctly stored and correctly loaded on subsequent timer-periods.

Loading the counter with 0 effectively stops the timer.

When starting the countdown timer for the first time, only the first period does not have a fixed duration. The amount of inaccuracy for the first timer-period depends on the chosen source clock, see next page table.

First period delay for timer counter value n:

Timer source clock	Minimum timer-period	Maximum timer-period
4.096 kHz	n	n + 1
64 Hz	n	n + 1
1 Hz	(n - 1) + $^1/_{64}$ Hz	n + $^1/_{64}$ Hz
$^1/_{60}$ Hz	(n - 1) + $^1/_{64}$ Hz	n + $^1/_{64}$ Hz
$^1/_{3600}$ Hz	(n - 1) + $^1/_{64}$ Hz	n + $^1/_{64}$ Hz

The generation of interrupts from the countdown timer is controlled via the CTAIE bit (register Control 2).

When the interrupt generation is enabled (CTAIE = 1) and the countdown timer flag CTAF is set logic 1, an interrupt signal on $\overline{\text{INT\_1}}$ is generated. The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal, which follows the condition of CTAF (register Control 2). The TAM bit (register Timer & CLKOUT) is used to control this mode selection. The interrupt output may be disabled with the CTAIE bit (register Control 2).

9.9.2.TIMER B

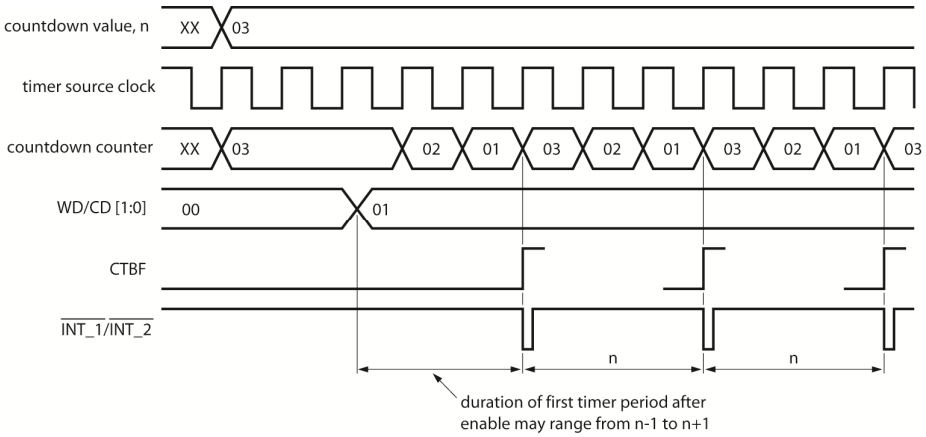
Timer B can only be used as a countdown timer and can be switched on and off by the TBC bit in register Timer & CLKOUT (0Fh).

The generation of interrupts from the countdown timer is controlled via the CTBIE bit (register Control 2).

When enabled, it counts down from the software programmed 8 bit binary value n in register Timer B (13h). When the counter reaches 1, on the next rising edge of the timer clock, the following events occur (see figure below):

- The countdown timer flag CTBF (register Control 2) is set logic 1
- When the interrupt generation is enabled (CTBIE = 1), interrupt signals on $\overline{\text{INT\_1}}$ and $\overline{\text{INT\_2}}$ are generated
- The counter automatically reloads
- The next timer-period starts

General countdown timer behavior:



In this example, it is assumed that the countdown timer flag (CTAF) is cleared before the next countdown period expires and that the interrupt output is set to pulse mode.

At the end of every countdown, the timer sets the countdown timer flag CTBF (register Control 2). CTBF may only be cleared by using the interface. Instructions, how to clear a flag, are given in section 9.5.

When reading the timer, the current countdown value is returned and **not** the initial value n. Since it is not possible to freeze the countdown timer counter during read back, it is recommended to read the register twice and check for consistent results.

If a new value of n is written before the end of the actual timer-period, this value will take immediate effect. It is not recommended to change n without first disabling the counter by setting TBC logic 0 (register Timer & CLKOUT). The update of n is asynchronous to the timer clock. Therefore changing it on the fly could result in a corrupted value loaded into the countdown counter. This can result in an undetermined countdown period for the first period. The countdown value n will be correctly stored and correctly loaded on subsequent timer-periods.

Loading the counter with 0 effectively stops the timer.

When starting the countdown timer for the first time, only the first period does not have a fixed duration. The amount of inaccuracy for the first timer-period depends on the chosen source clock; see section 9.9.1.

When the interrupt generation is enabled (CTBIE = 1) and the countdown timer flag CTAF is set logic 1, interrupt signals on $\overline{\text{INT\_1}}$ and $\overline{\text{INT\_2}}$ are generated. The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal, which follows the condition of CTBF (register Control 2). The TBM bit (register Timer & CLKOUT) is used to control this mode selection. Interrupt output may be disabled with the CTBIE bit (register Control 2).

9.9.3.SECOND INTERRUPT TIMER

The RV-8523 has a pre-defined timer, which is used to generate an interrupt once per second. The pulse generator for the second interrupt timer operates from an internal 64 Hz clock and generates a pulse of $^1/_{64}$ s in duration. It is independent of the watchdog or countdown timer and can be switched on and off by the SIE bit in register Control 1 (00h).

The interrupt generated by the second interrupt timer may be generated as pulsed signal every second or as a permanently active signal. The TAM bit (register Timer & CLKOUT) is used to control the interrupt generation mode.

When the second interrupt timer is enabled (SIE = 1), then the timer sets the flag SF (register Control 2) every second (see table below). SF may only be cleared by using the interface. Instructions, how to clear a flag, are given in section 9.5.

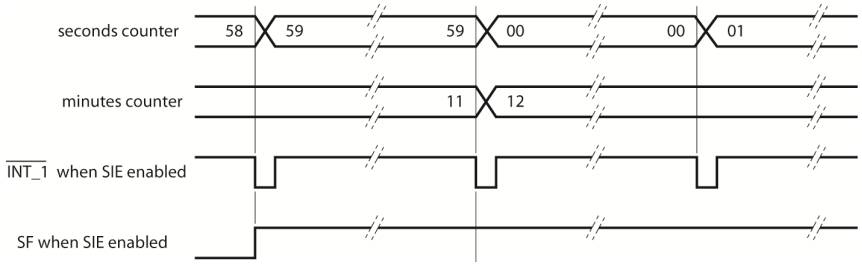
Effect of bit SIE on $\overline{\text{INT\_1}}$ and bit SF:

SIE	**Result on $\overline{\text{INT\_1}}$**	**Result on SF**
0	No interrupt generated	SF never set
1	An interrupt once per second	SF set when **seconds** counter increments

When SF is logic 1:

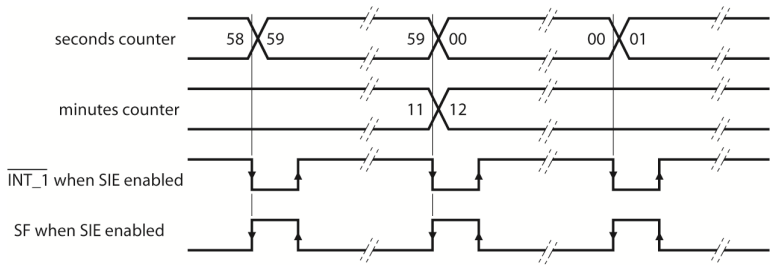
- If TAM (register Timer & CLKOUT) is logic 1, the interrupt is generated as a pulsed signal every second
- If TAM is logic 0, the interrupt is a permanently active signal that remains, until SF is cleared

Example for second interrupt when TAM = 1:



In this example, bit TAM is set logic 1 and SF flag is not cleared after an interrupt.

Example for second interrupt when TAM = 0:



In this example, bit TAM is set logic 0 and SF flag is cleared after an interrupt.

9.9.4.TIMER INTERRUPT PULSE

The timer interrupt is generated as a pulsed signal when TAM or TBM are set logic 1. The pulse generator for the timer interrupt also uses an internal clock, but this time it is dependent on the selected source clock for the timer and on the timer register value n. So, the width of the interrupt pulse varies; see tables below.

Interrupt low pulse width for timer A (pulse mode, bit TAM set logic 1):

Source clock (Hz)	**Interrupt pulse width**	
	n = 1[1)]	**n > 1**[1)]
4096	122 µs	244 µs
64	7.812 ms	15.625 ms
1	15.625 ms	15.625 ms
$^1/_{60}$	15.625 ms	15.625 ms
$^1/_{3600}$	15.625 ms	15.625 ms

[1)] n = loaded timer register value. Timer stops when n = 0.

For timer B, interrupt pulse width is programmable via bit TBM (register Timer & CLKOUT).

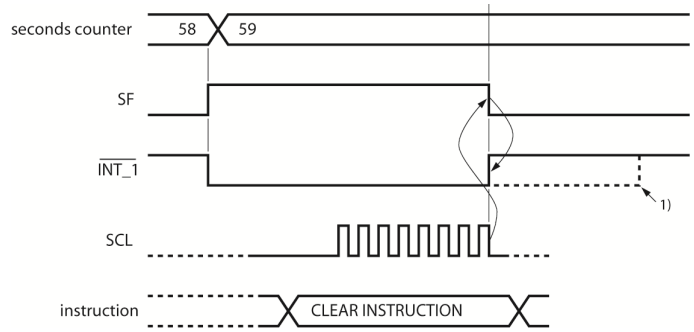
Interrupt low pulse width for timer B (pulse mode, bit TBM set logic 1):

Source clock (Hz)	**Interrupt pulse width**	
	n = 1[1)]	**n > 1**[1)]
4096	122 µs	244 µs
64	7.812 ms	See section 8.6.4.[2)]
1	See section 8.6.4.	:
$^1/_{60}$	:	:
$^1/_{3600}$	:	:

[1)] n = loaded timer register value. Timer stops when n = 0.
[2)] If pulse period is shorter than the setting via bit TBW[2:0], the interrupt pulse width is set to 15.625 ms.

When flags like SF, CTAF, WTAF and CTBF are cleared before the end of the interrupt pulse, then the interrupt pulse is shortened. This allows the source of a system interrupt to be cleared immediately when it is serviced, that is, the system does not have to wait for the completion of the pulse before continuing; see figures below. Instructions for clearing flags can be found in section 9.5. Instructions for clearing the bit WTAF can be found in section 9.9.1.

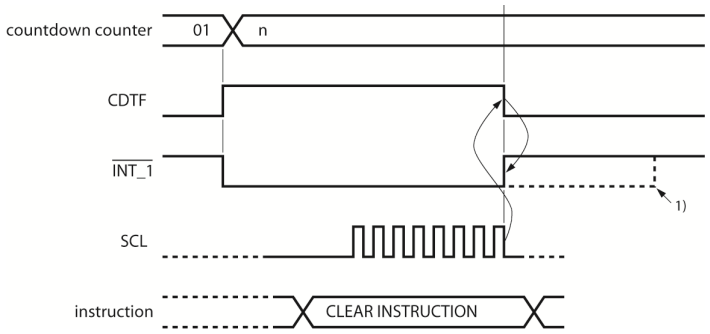
Example of shortening the $\overline{\text{INT\_1}}$ pulse by clearing the SF flag:



The timing shown for clearing bit SF is also valid for the non-pulsed interrupt mode, that is, when TAM set logic 0, where the $\overline{\text{INT\_1}}$ pulse may be shortened by setting SIE logic 0.

[1)] Indicates normal duration of $\overline{\text{INT\_1}}$ pulse.

Example of shortening the $\overline{INT\_1}$ pulse by clearing the CTAF flag:



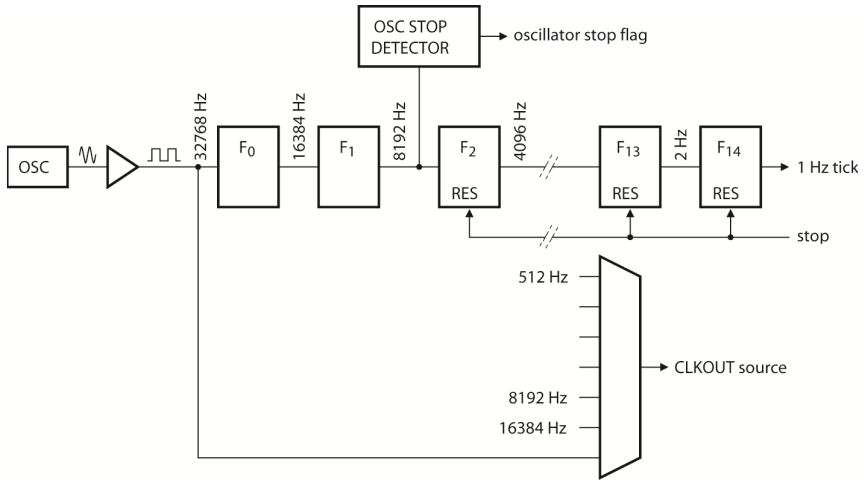
The timing shown for clearing bit CTAF is also valid for the non-pulsed interrupt mode, that is, when TAM set logic 0, where the $\overline{INT\_1}$ pulse may be shortened by setting CTAIE logic 0.

[1] Indicates normal duration of $\overline{INT\_1}$ pulse.

9.10. STOP BIT FUNCTION

The STOP bit function allows the accurate starting of the time circuits. The STOP bit function causes the upper part of the prescaler (F_2 to F_{14}) to be held in reset and thus no 1 Hz ticks are generated. The time circuits can then be set and do not increment until the STOP bit is released (see figure below).

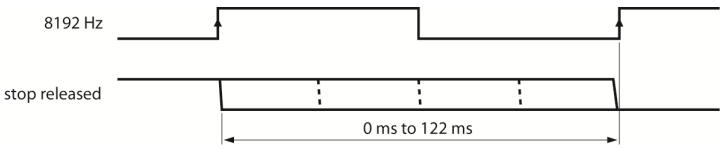
STOP bit:



STOP does not affect the output of 32.768 kHz, 16.384 kHz or 8.192 kHz (see section 8.6.1.).

The lower two stages of the prescaler (F_0 and F_1) are not reset and because the I^2C bus interface is asynchronous to the crystal oscillator, the accuracy of re-starting the time circuits will be between 0 and one 8.192 kHz cycle (see figure below).

STOP bit release timing:



The first increment of the time circuits is between 0.499878 s and 0.500000 s after STOP is released. The uncertainty is caused by the prescaler bits F_0 and F_1 not being reset (see table below).

First increment of the time circuits after STOP release:

Bit	**Prescaler bits**[1)]	**1 Hz Tick**	**Time**	**Comment**
STOP	**F_0F_1-F_2 to F_{14}**		**hh:mm:ss**	
Clock is running normally				
0	01-0000111010100		12:45:12	Prescaler counting normally
STOP bit is activated by user; F_0 and F_1 are not reset and values cannot be predicted externally				
1	XX-0000000000000		12:45:12	Prescaler is reset; time circuits are frozen
New time is set by user				
1	XX-0000000000000		08:00:00	Prescaler is reset; time circuits are frozen
STOP is released by user				
0	XX-0000000000000	0.499878 s to 0.500000 s	08:00:00	Prescaler is now running
0	XX-1000000000000		08:00:00	-
0	XX-0100000000000		08:00:00	-
0	XX-1100000000000		08:00:00	-
:	:		:	:
0	11-1111111111110		08:00:00	-
0	00-0000000000001		08:00:01	0 to 1 transition of F_{14} increments the time circuits
0	10-0000000000001		08:00:01	-
:	:	1 s	:	:
0	11-1111111111111		08:00:01	-
0	00-0000000000000		08:00:01	-
:	:		:	-
0	11-1111111111110		08:00:01	-
0	00-0000000000001		08:00:02	0 to 1 transition of F_{14} increments the time circuits

[1)] F_0 is clocked at 32.768 kHz.

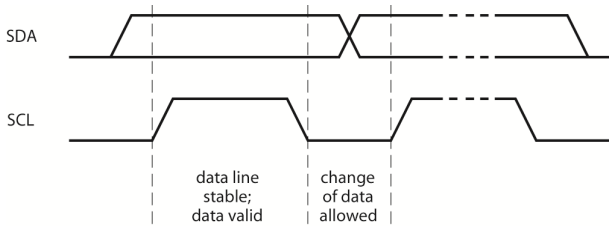
10. CHARACTERISTICS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines are connected to a positive supply via pull-up resistors. Data transfer is initiated only when the bus is not busy.

10.1. BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line remains stable during the HIGH period of the clock pulse, as changes in the data line at this time are interpreted as a control signals. Data changes should be executed during the LOW period of the clock pulse (see figure below).

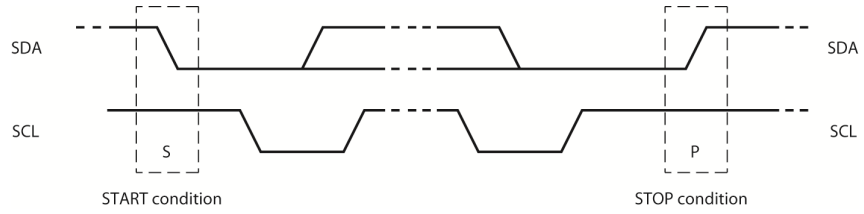
Bit transfer:



10.2. START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the STOP condition (P) (see figure below).

Definition of START and STOP conditions:



For this device, a repeated START is not allowed. Therefore, a STOP has to be released before the next START.

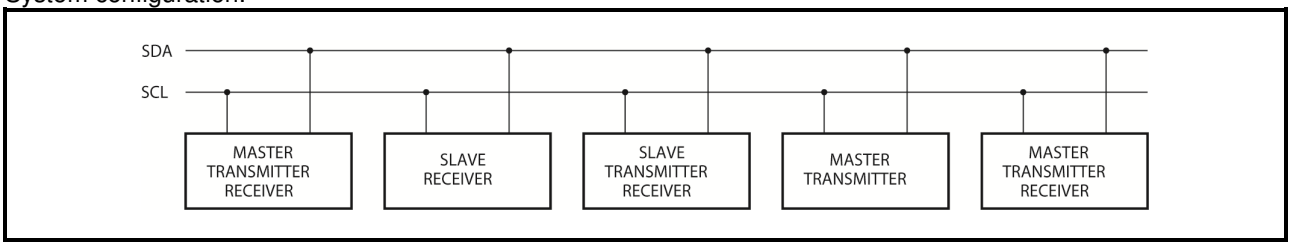
10.3. SYSTEM CONFIGURATION

Since multiple devices can be connected with the I^2C bus, all I^2C bus devices have a fixed and unique device number built-in to allow individual addressing of each device.

The device that controls the I^2C bus is the Master; the devices which are controlled by the Master are the Slaves. A device generating a message is a Transmitter; a device receiving a message is the Receiver. The RV-8523 acts as a Slave-Receiver or Slave-Transmitter.

Before any data is transmitted on the I^2C bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

System configuration:



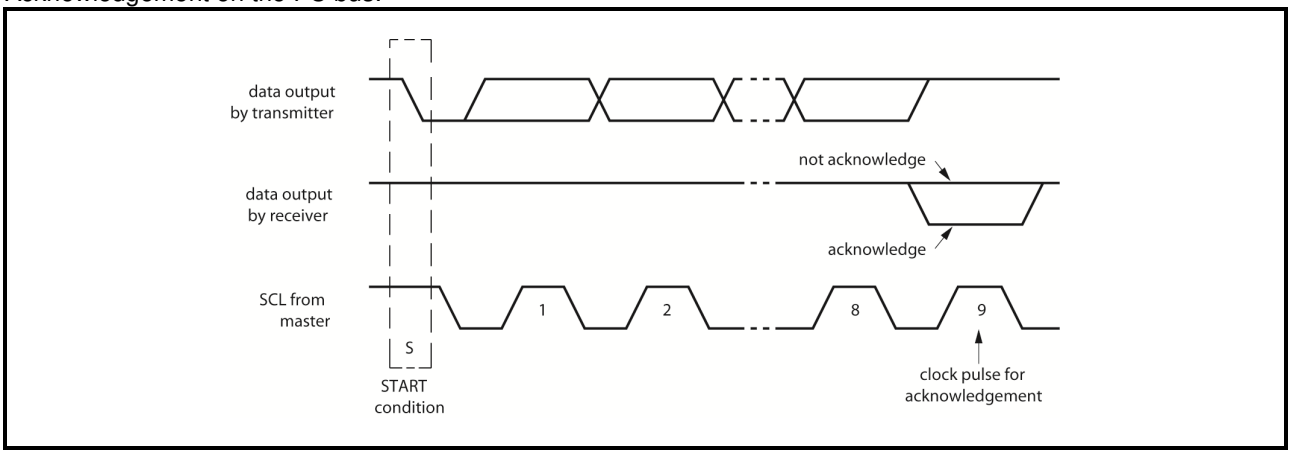
10.4. ACKNOWLEDGE

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge cycle after the reception of each byte
- Also a master receiver must generate an acknowledge cycle after the reception of each byte that has been clocked out of the slave transmitter
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the related acknowledge clock pulse (set-up and hold times must be considered)
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge cycle on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition

Acknowledgement on the I^2C bus is shown on the figure below.

Acknowledgement on the I^2C bus:



11.I²C BUS PROTOCOL

11.1. ADDRESSING

One I²C bus slave address (1101000) is reserved for the RV-8523. The entire I²C bus slave address byte is shown in the table below:

I²C salve address byte:

Bit	Slave address							
	7 MSB	**6**	**5**	**4**	**3**	**2**	**1**	**0 LSB**
	1	1	0	1	0	0	0	R/$\overline{W}$

After a START condition, the I²C slave address has to be sent to the RV-8523 device.

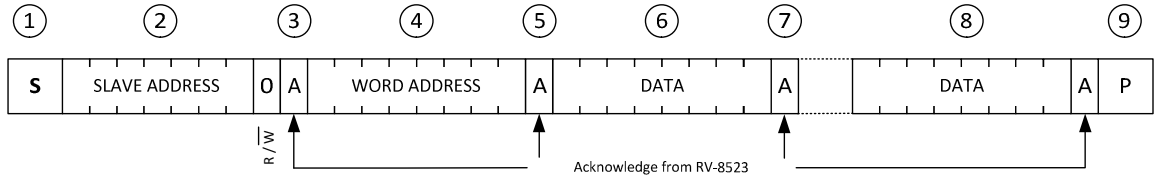
The R/$\overline{W}$ bit defines the direction of the following single or multiple byte data transfer. In the write mode, a data transfer is terminated by sending either the STOP condition or the START condition of the next data transfer.

11.2. CLOCK AND CALENDAR READ AND WRITE CYCLES

11.2.1. WRITE MODE

Master transmits to Slave-Receiver at specified address. The Word Address is 4-bit value that defines which register is to be accessed next. The upper four bits of the Word Address are not used. After reading or writing one byte, the Word Address is automatically incremented by 1.

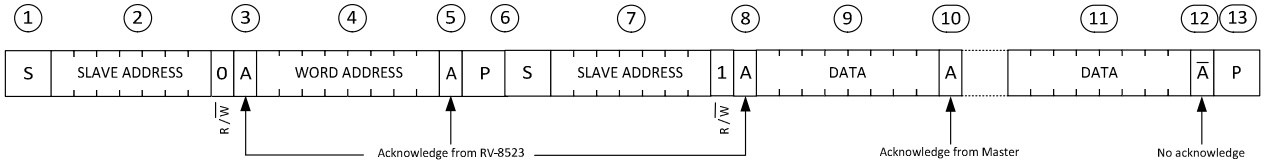
1) Master sends out the “Start Condition”.
2) Master sends out the “Slave Address”, D0h for the RV-8523; the R/$\overline{W}$ bit in write mode.
3) Acknowledgement from the RV-8523.
4) Master sends out the “Word Address” to the RV-8523.
5) Acknowledgement from the RV-8523.
6) Master sends out the “data” to write to the specified address in step 4).
7) Acknowledgement from the RV-8523.
8) Steps 6) and 7) can be repeated if necessary. The address will be incremented automatically in the RV-8523.
9) Master sends out the “Stop Condition”.



11.2.2. READ MODE AT SPECIFIC ADDRESS

Master reads data after setting Word Address:

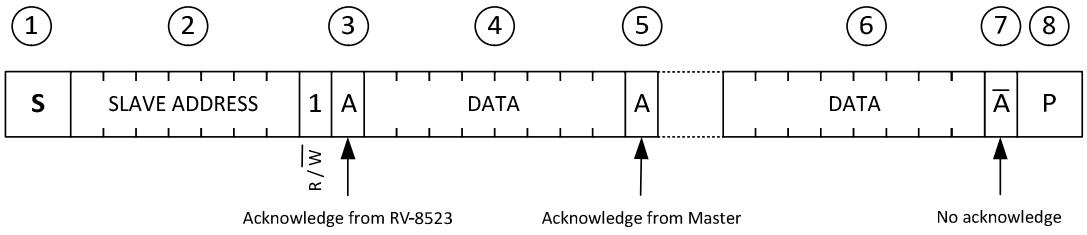
1) Master sends out the “Start Condition”.
2) Master sends out the “Slave Address”, D0h for the RV-8523; the R/$\overline{W}$ bit in write mode.
3) Acknowledgement from the RV-8523.
4) Master sends out the “Word Address” to the RV-8523.
5) Acknowledgement from the RV-8523.
6) Master sends out the “Re-Start Condition” (“Stop Condition” followed by “Start Condition”)
7) Master sends out the “Slave Address”, D1h for the RV-8523; the R/$\overline{W}$ bit in read mode.
8) Acknowledgement from the RV-8523.
   At this point, the Master becomes a Receiver, the Slave becomes the Transmitter.
9) The Slave sends out the “data” from the Word Address specified in step 4).
10) Acknowledgement from the Master.
11) Steps 9) and 10) can be repeated if necessary.
    The address will be incremented automatically in the RV-8523.
12) The Master, addressed as Receiver, can stop data transmission by not generating an acknowledge on the last byte that has been sent from the Slave-Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a stop condition.
13) Master sends out the “Stop Condition”.



11.2.3. READ MODE

Master reads Slave-Transmitter immediately after first byte:

1) Master sends out the “Start Condition”.
2) Master sends out the “Slave Address”, D1h for the RV-8523; the R/$\overline{W}$ bit in read mode.
3) Acknowledgement from the RV-8523.
   At this point, the Master becomes a Receiver, the Slave becomes the Transmitter
4) The RV-8523 sends out the “data” from the last accessed Word Address incremented by 1.
5) Acknowledgement from the Master.
6) Steps 4) and 5) can be repeated if necessary.
   The address will be incremented automatically in the RV-8523.
7) The Master, addressed as Receiver, can stop data transmission by not generating an acknowledge on the last byte that has been sent from the Slave-Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a stop condition.
8) Master sends out the “Stop Condition”.



12. ABSOLUTE MAXIMUM RATING

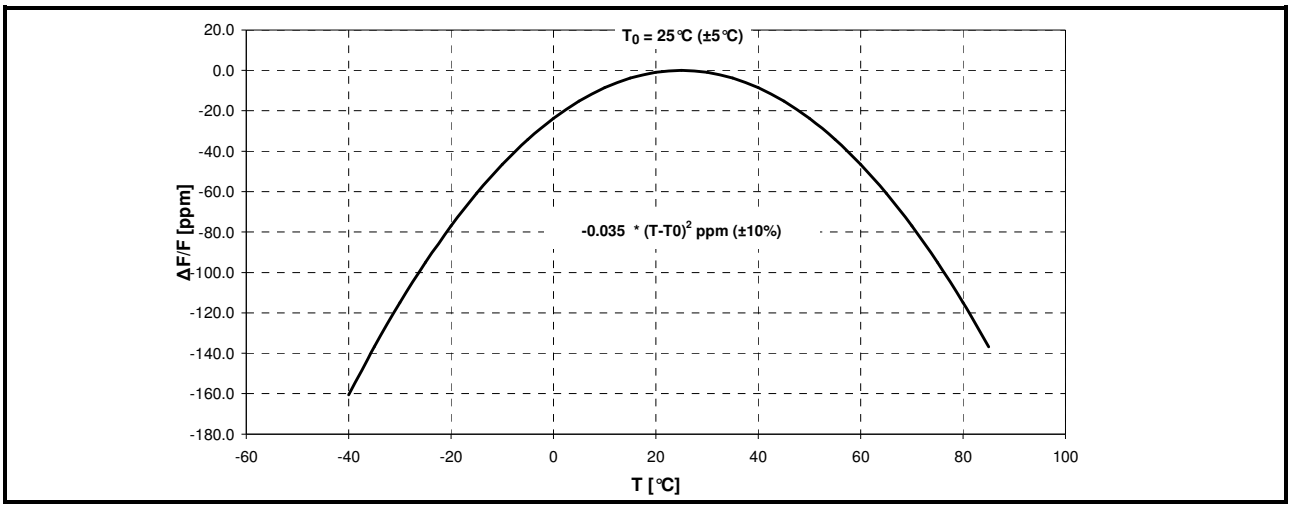
PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT
Supply voltage	V_{DD}		-0.5	+6.5	V
Battery supply voltage	V_{BACKUP}		-0.5	+6.5	V
Input voltage	V_I		-0.5	+6.5	V
Output voltage	V_O		-0.5	+6.5	V
Supply current	I_{DD}		-50	+50	mA
DC Input current	I_I		-10	+10	mA
DC Output current	I_O		-10	+10	mA
Electrostatic discharge voltage	V_{ESD}	HBM[1)]	-	+/-2000	V
		CDM[2)]	-	+/-1500	V
Latch-up current	I_{LU}	[3)]	-	100	mA
Operating temperature range	T_{OPR}		-40	+85	°C
Storage temperature range	T_{STO}	Stored as bare product	-55	+125	°C

[1)] Pass level; Human Body Model (HBM), according to JESD22-A114.
[2)] Pass level; Charged-Device Model (CDM), according to JESD22-C101.
[3)] Pass level; latch-up testing, according to JESD78 at maximum ambient temperature ($T_{amb(max)}$ = +85°C).

13. FREQUENCY CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	TYP.	MAX.	UNIT
Frequency precision	ΔF/F	T_{AMB} = +25°C V_{DD} = 3.0 V	+/-10	+/-20	ppm
Frequency vs. voltage characteristics	ΔF/V	T_{AMB} = +25°C V_{DD} = 1.8 V to 5.5 V	+/-0.8	+/-1.5	ppm/V
Frequency vs. temperature characteristics	$\Delta F/F_{OPR}$	T_{REF} = +25°C V_{DD} = 3.0 V	$-0.035^{ppm}/_{°C^2}$ $(T_{OPR}-T_O)^2$ +/-10%		ppm
Turnover temperature	T_0		+25	+/-5	°C
Aging first year max.	V_O ΔF/F	At 25°C		+/-3	ppm
Oscillator start-up time	T_{START}	At 25°C	350	500	ms
CLKOUT duty cycle	δ_{CLKOUT}	At 25°C	50	40/60	%

13.1. FREQUENCY VS. TEMPERATURE CHARACTERISTICS



14. DC CHARACTERISTICS

V_{DD} = 1.2 V to 5.5 V; V_{SS} = 0 V; T_{AMB} = -40°C to +85°C; f_{OSC} = 32.768 kHz; unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power Supply Voltage						
Supply voltage	V_{DD}	For clock data integrity I^2C bus inactive	1.2	-	5.5	V
		I^2C bus active	1.6	-	5.5	V
		Power management function active	1.8	-	5.5	V
Slew rate	SR	Of V_{DD}	-	-	+/-0.5	V/ms
Battery supply voltage	V_{BACKUP}	Power management function active	1.8	-	5.5	V
Power Supply Current						
Current consumption I^2C bus active	I_{DD}	f_{SCL} = 1000 kHz V_{DD} = 3.0 V	-	100	200	µA
		f_{SCL} = 100 kHz V_{DD} = 3.0 V	-	50	100	µA
Current consumption[1)] I^2C bus inactive (f_{SCL} = 0 Hz) Interrupts disabled CLKOUT disabled Power management fct. disabled (PM[2:0] = 111) T_{AMB} = 25°C	I_{DDO}	V_{DD} = 3.0 V	-	130	180	nA
		V_{DD} = 2.0 V	-	110	160	nA
Current consumption[1)] I^2C bus inactive (f_{SCL} = 0 Hz) Interrupts disabled CLKOUT disabled Power management fct. disabled (PM[2:0] = 111) T_{AMB} = -40 to +85°C	I_{DDO}	V_{DD} = 2.0 to 5.0 V	-	-	500	nA
Current consumption[2)] I^2C bus inactive (f_{SCL} = 0 Hz) Interrupts disabled CLKOUT enabled (32.768 kHz) Power management fct. enabled (PM[2:0] = 000) T_{AMB} = 25°C	I_{DD32k}	V_{BACKUP} or V_{DD} = 3.0 V	-	1200	-	nA
Current consumption[2)] I^2C bus inactive (f_{SCL} = 0 Hz) Interrupts disabled CLKOUT enabled (32.768 kHz) Power management fct. enabled (PM[2:0] = 000) T_{AMB} = -40 to +85°C	I_{DD32k}	V_{BACKUP} or V_{DD} = 2.0 to 5.0 V	-	-	3600	nA
Battery leakage current	$I_{L(bat)}$	V_{DD} active; V_{BACKUP} = 3.0 V	-	50	100	nA
Power Management						
Battery switch threshold voltage	$V_{th(sw)bat}$		2.28	2.5	2.7	V

V_{DD} = 1.2 V to 5.5 V; V_{SS} = 0 V; T_{AMB} = -40°C to +85°C; f_{OSC} = 32.768 kHz; unless otherwise specified

Inputs[3]						
LOW level input voltage	V_{IL}		-	-	30% V_{DD}	V
HIGH level input voltage	V_{IH}		70% V_{DD}	-	-	V
Input voltage	V_I		-0.5	-	V_{DD} +0.5	V
Input leakage current	I_{LI}	$V_I = V_{DD}$ or V_{SS}	-	0	-	nA
		Post ESD event	-1	-	+1	µA
Input capacitance[4]	C_I		-	-	7	pF
Outputs						
Output voltage	V_O	On pins $\overline{INT\_1}$, $\overline{INT\_2}$, CLKOUT, SDA (refers to ext. pull-up voltage)	-0.5	-	5.5	V
LOW level output voltage	V_{OL}		V_{SS}	-	0.4	V
LOW level output current[5]	I_{OL}	Output sink current; On pins $\overline{INT\_1}$, $\overline{INT\_2}$, CLKOUT V_{OL} = 0.4 V; V_{DD} = 5.0 V	1.5	-	-	mA
		On pin SDA V_{OL} = 0.4 V; V_{DD} = 3.0 V	20	-	-	mA
Output leakage current	I_{LO}	$V_O = V_{DD}$ or V_{SS}	-	0	-	nA
		Post ESD event	-1	-	+1	µA

[1] Timer source clock = $^1/_{3600}$ Hz, level of pins SCL and SDA is V_{DD} or V_{SS}.
[2] When the device is supplied via the V_{BACKUP} pin instead of the V_{DD} pin, the current values for I_{BACKUP} will be as specified for I_{DD} under the same conditions.
[3] The I^2C bus is 5 V tolerant.
[4] Implicit by design.
[5] Tested on sample basis.

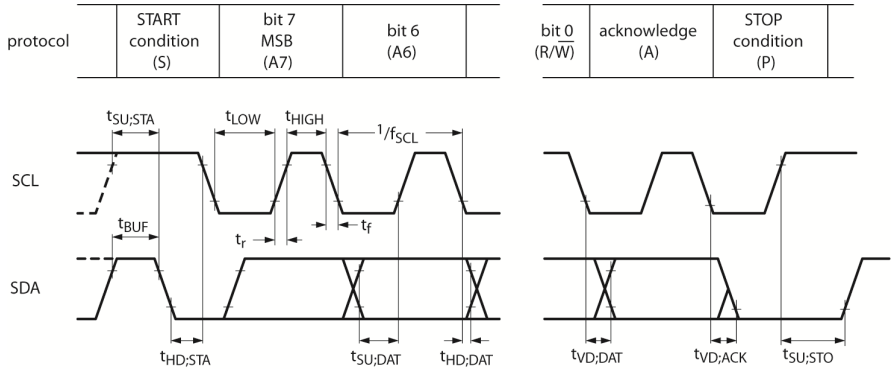
15.I²C BUS INTERFACE TIMING

All timing characteristics are valid within the operating supply voltage and ambient temperature range and reference to 30% and 70% with an input voltage swing of V_{SS} to V_{DD} (see figure below).

PARAMETER	SYMBOL	STANDARD MODE		FAST MODE (FM)		FAST MODE PLUS (FM+)[1]		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Pin SCL								
SCL clock frequency[2]	f_{SCL}	-	100	-	400	-	1000	kHz
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	0.5	-	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	0.26	-	µs
Pin SDA								
Data setup time	$t_{SU;DAT}$	250	-	100	-	50	-	ns
Data hold time	$t_{HD;DAT}$	0	-	0	-	0	-	ns
Pins SCL and SDA								
Bus free time between STOP and START condition	t_{BUF}	4.7	-	1.3	-	0.5	-	µs
Setup time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	0.26	-	µs
Hold time (repeated) START condition	$t_{HD;STA}$	4.0	-	0.6	-	0.26	-	µs
Setup time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	0.26	-	µs
Rise time of both SDA and SCL signals[3] [4]	t_r	-	1000	$20+0.1C_b$	300	-	120	ns
Fall time of both SDA and SCL signals[3] [4]	t_f	-	300	$20+0.1C_b$	300	-	120	ns
Capacitive load for each bus line	C_b	-	400	-	400	-	550	pF
Data valid acknowledge time[5]	$t_{VD;ACK}$	-	3.45	-	0.9	-	0.45	µs
Data valid time[6]	$t_{VD;DAT}$	-	3.45	-	0.9	-	0.45	µs
Pulse width of spikes that must be suppressed by the input filter[7]	t_{SP}	-	50	-	50	-	50	ns

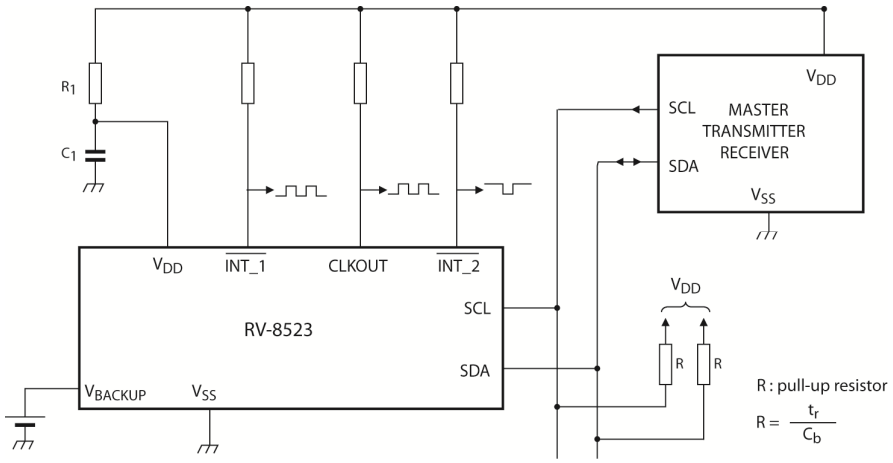
[1] Fast mode plus guaranteed at 3.0 V < V_{DD} < 5.5 V.
[2] The minimum SCL clock frequency is limited by the bus time-out feature, which resets the serial bus interface if either the SDA or SCL is held LOW for a minimum of 25 ms. The bus time-out feature must be disabled for DC operation.
[3] A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
[4] The maximum t_f for the SDA and SCL bus lines is 300 ns. The maximum fall time for the SDA output stage, t_f is 250 ns. This allows series protection resistors to be connected between the SDA pin, the SCL pin and the SDA/SCL bus lines without exceeding the maximum t_f.
[5] $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA output LOW.
[6] $t_{VD;DAT}$ = minimum time for valid SDA output following SCL LOW.
[7] Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.

15.1. TIMING DIAGRAM



Rise and fall times refer to 30% and 70%.

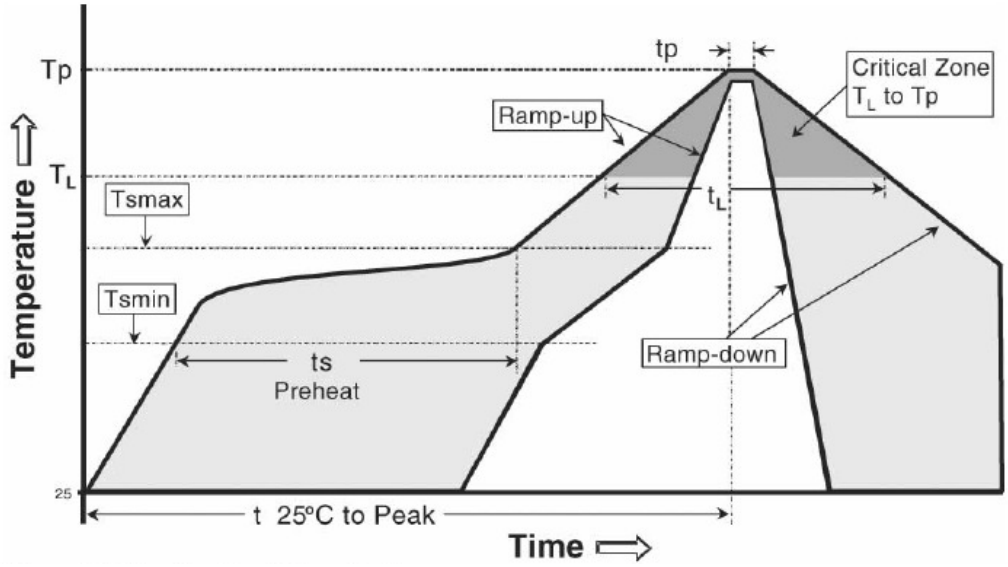
16. APPLICATION DIAGRAM



R_1 and C_1 are recommended to limit the slew rate (SR, see section 14.) of V_{DD}. If V_{DD} drops to fast, the internal supply switch to the battery is not guaranteed.

17. RECOMMENDED REFLOW TEMPERATURE (LEADFREE SOLDERING)

Maximum Reflow Conditions in accordance with IPC/JEDEC J-STD-020C "Pb-free"



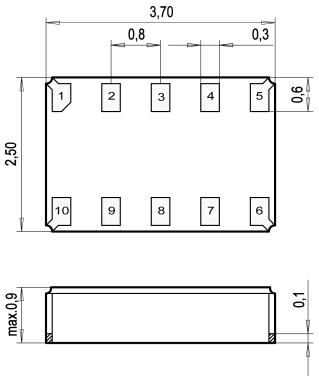
Temperature Profile	Symbol	Condition	Unit
Average ramp-up rate	(Ts_{max} to Tp)	3°C / second max	°C / s
Ramp down Rate	T_{cool}	6°C / second max	°C / s
Time 25°C to Peak Temperature	$T_{to\text{-}peak}$	8 minutes max	m
Preheat			
Temperature min	Ts_{min}	150	°C
Temperature max	Ts_{max}	200	°C
Time Ts_{min} to Ts_{max}	ts	60 - 180	Sec
Soldering above liquidus			
Temperature liquidus	T_L	217	°C
Time above liquidus	t_L	60 – 150	sec
Peak temperature			
Peak Temperature	Tp	260	°C
Time within 5°C of peak temperature	tp	20 - 40	sec

18. PACKAGE

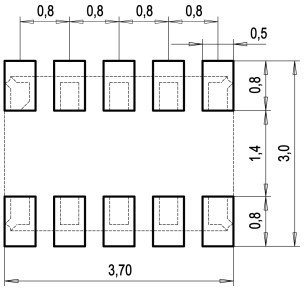
18.1. DIMENSIONS AND SOLDERPADS LAYOUT

C3 Package:

Package dimensions (bottom view):



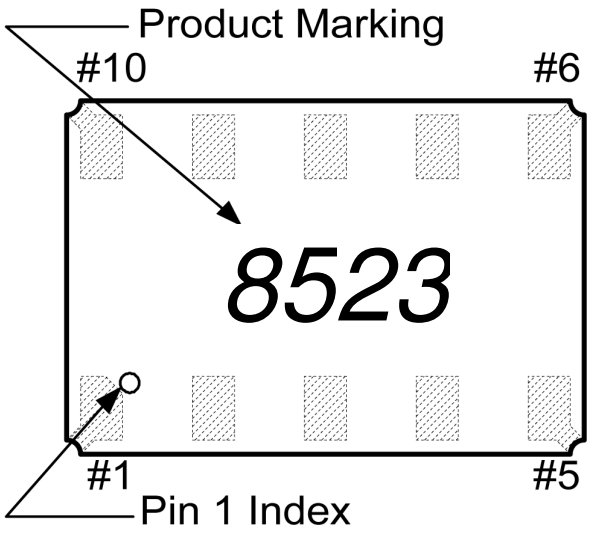
Recommended solderpad layout:



All dimensions in mm typical.

18.2. MARKING AND PIN #1 INDEX

C3 Package:

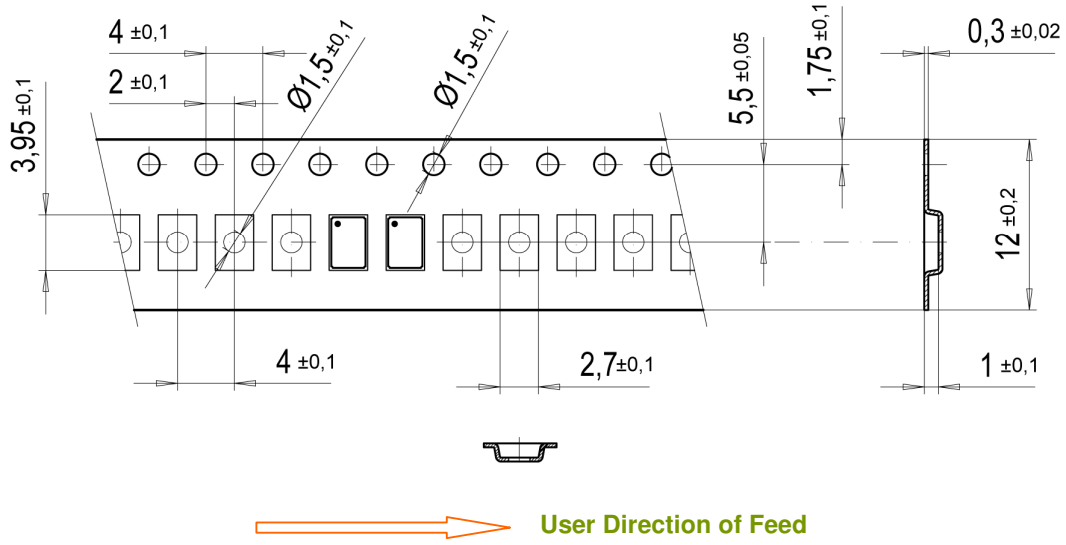


19. PACKING INFORAMTION

19.1. CARRIER TAPE

12 mm Carrier-Tape:	Material:	Polystyrene / Butadine or Polystyrol black, conductive
Cover Tape:	Base Material:	Polyester, conductive 0.061 mm
	Adhesive Material:	Pressure-sensitive Synthetic Polymer

C3 Package:



Tape Leader and Trailer: 300 mm minimum.
All dimensions in mm.

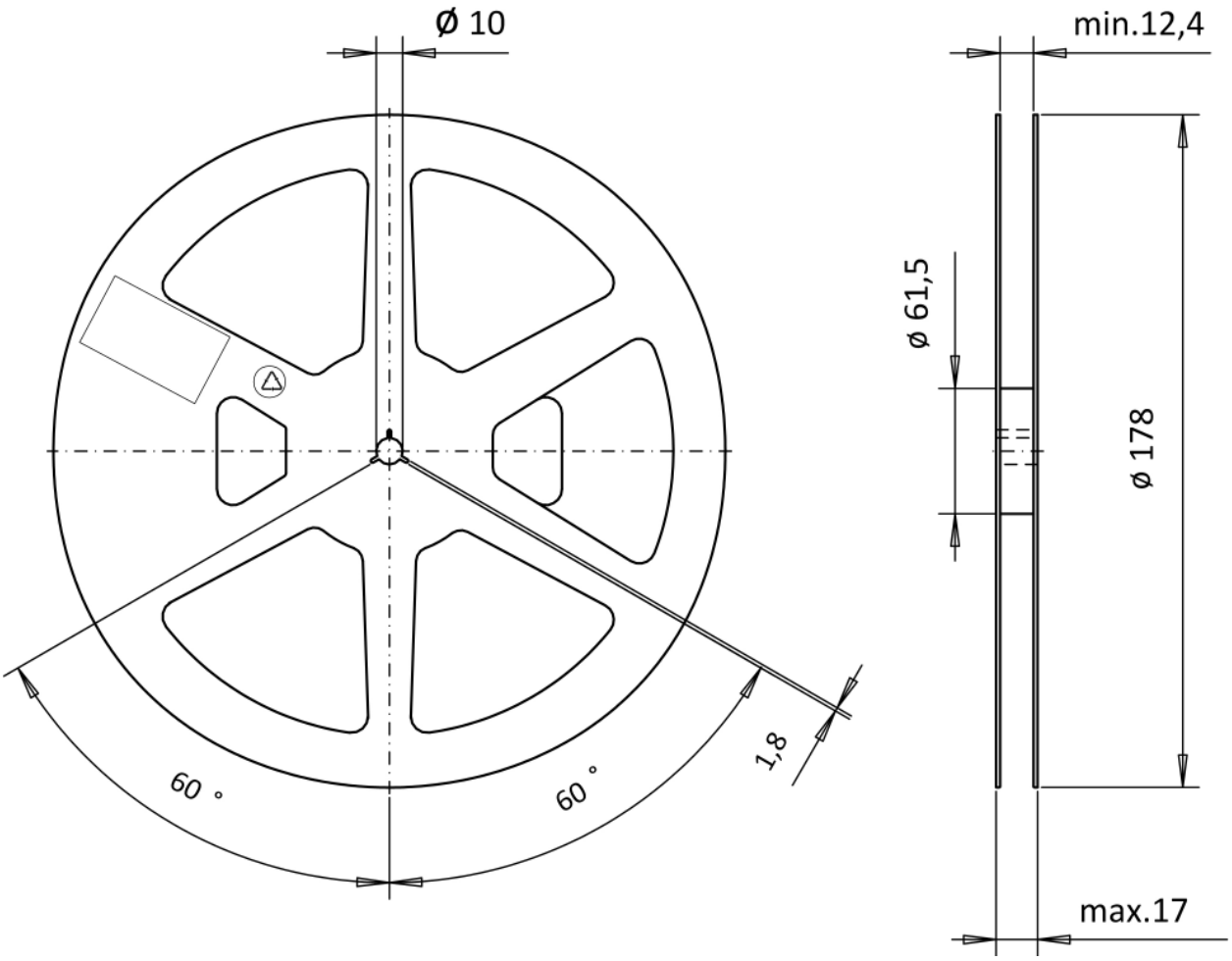
19.2. PARTS PER REEL

C3 Package:

Reels:

Diameter	Material	RTC's per reel
7"	Plastic, Polystyrol	1'000
7"	Plastic, Polystyrol	3'000

19.3. REEL 7 INCH FOR 12 mm TAPE



Reel:

Diameter	Material
7”	Plastic, Polystyrol

20. HANDLING PRECAUTIONS FOR CRYSTALS OR MODULES WITH EMBEDDED CRYSTALS

The built-in tuning-fork crystal consists of pure Silicon Dioxide in crystalline form. The cavity inside the package is evacuated and hermetically sealed in order for the crystal blank to function undisturbed from air molecules, humidity and other influences.

Shock and vibration:

Keep the crystal / module from being exposed to **excessive mechanical shock and vibration**. Micro Crystal guarantees that the crystal / module will bear a mechanical shock of 5000g / 0.3 ms.

The following special situations may generate either shock or vibration:

Multiple PCB panels - Usually at the end of the pick & place process the single PCBs are cut out with a router. These machines sometimes generate vibrations on the PCB that have a fundamental or harmonic frequency close to 32.768 kHz. This might cause breakage of crystal blanks due to resonance. Router speed should be adjusted to avoid resonant vibration.

Ultrasonic cleaning - Avoid cleaning processes using ultrasonic energy. These processes can damages crystals due to mechanical resonance of the crystal blank.

Overheating, rework high temperature exposure:

Avoid overheating the package. The package is sealed with a seal ring consisting of 80% Gold and 20% Tin. The eutectic melting temperature of this alloy is at 280°C. Heating the seal ring up to >280°C will cause melting of the metal seal which then, due to the vacuum, is sucked into the cavity forming an air duct. This happens when using hot-air-gun set at temperatures >300°C.

Use the following methods for rework:

- Use a hot-air- gun set at 270°C.
- Use 2 temperature controlled soldering irons, set at 270°C, with special-tips to contact all solder-joints from both sides of the package at the same time, remove part with tweezers when pad solder is liquid.

21. DOCUMENT REVISION HISTORY

Date	Revision #	Revision Details
January 2013	1.0	First release